

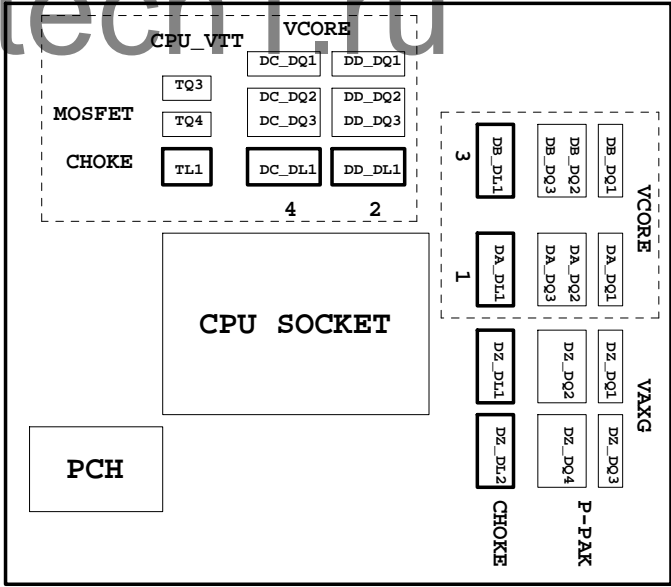
Model Name: GA-H77-D3H-MVP 1.02

SHEET TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1155-A
05	CPU_LGA1155-B
06	CPU_LGA1155-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE,NVRAM
10	PCH_DP,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCIEX1*3 , PCIEX4 SLOT
16	ITE8892 PCI BRIDGE
17	PCI SLOT 1&2
18	I/O ITE8728
19	COM, -PROHOT, R_USB
20	Dual BIOS , TPM SLB9635TT
21	VT2021 CODEC
22	REAR AUDIO JACK
23	VCORE PWM_IR3564
24	VCORE PWM DRIVER IR3598
25	NCP3933 OVER VOLTAGE
26	DISCRETE POWER
27	DDR_15V & CPU_VTT PWM IR3570

SHEET TITLE

28	DDR_15V & CPU_VTT PWM DRIVER CHL8550
29	VCCSA POWER
30	F_PANEL , F_USB2.0/3.0
31	ATX POWER, CLOCK GEN
32	HWM , KB/MS , FAN CTRL
33	LAN ATHEROS AR8151
34	N/A
35	M-SATA
36	DVI
37	HDMI , R_USB30
38	TABLE LIST
39	
40	



GA-H77-D3H-MVP

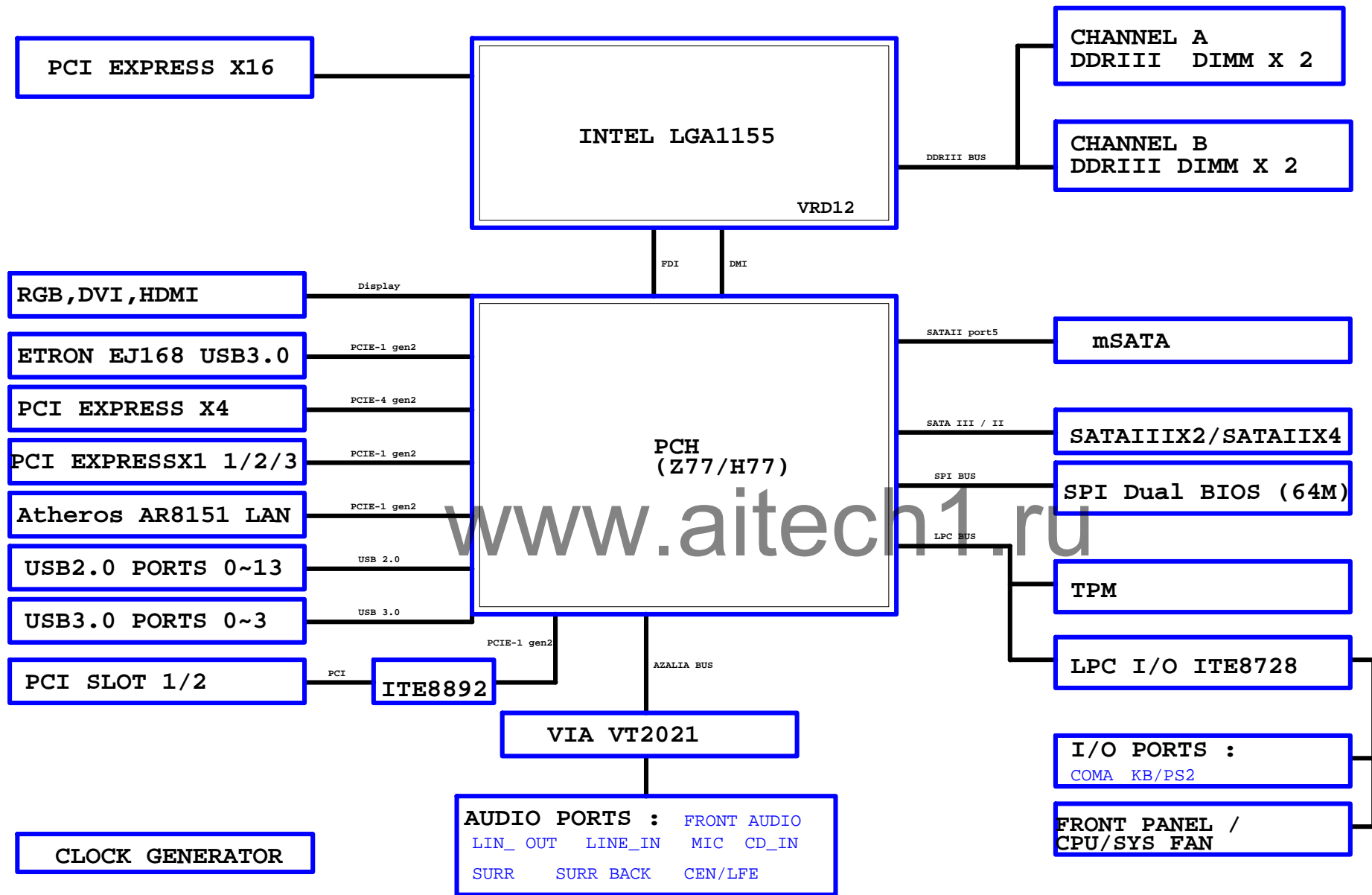
Component value change history

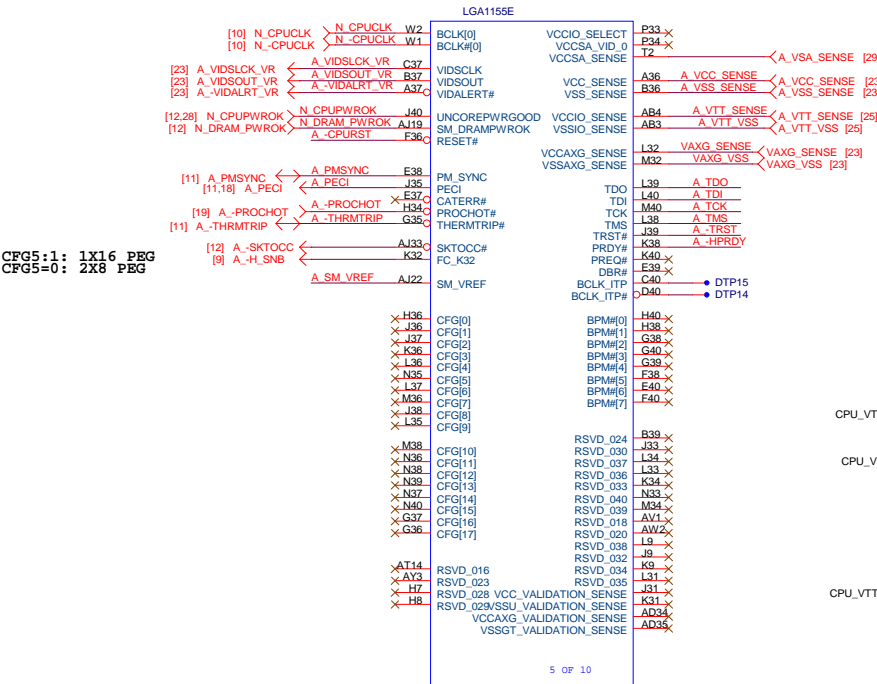
Data	Change Item	Reason
0.1-1124	E-BOM	
02-1216	1. ADD PCH_HS & MOS_HS料號	
	2. PCIE gen2 switch PI3PCIE2415ZHE --> ASM1440	
	3. load-line DAR5=12K , DAR40=1.78K	
10A-0105	1. Z77料號更新	
	2. PWM Driver power vcc or +12v?	
	3. DART2 --> 47K/1/4/S , DAR44 --> 0 ohm	
10B-0113	1. Vcore & VAXG VSEN modify , DAR1,DAR51=100/4/1,DAR2,DAR54=0/4,DAC1,DAC24=3.3mF	
	2. 1.54K加替料:10RC4-001541-22R TA-I	
	1. Remove IR PWM 1X3 pin	
10C-0117	1. DA_DR11,DC_DR11,DZ_DR18 1ohm --> 0ohm	
10D-0119	1. Prochot R65 : 1.65K/4/1 --> 2.74K/4/1	
10E-EVT-0201	1. Modify choke=0.36uH , DRIVER=5V	
10F	1. IR3564要改用新料號03R	
	2. poochot change 100K	
10E-ECN	1. ADD PCB:依利安達	
10T	1. 0 OHM Short-pad	
	2. DDR3 FOR OC 2400MHz UP	
10G	0. PCB Rev1.0 --> ReV1.01	
	1. RS_PWM相關線路移除 (若有上prochot pull up改100 ohm)	
	2. Add M/B ID for DDR3 OC	
	3. 固態電容區分100uF/6.3V & 100uF/16V	
H77-D3H-MVP		
10A-0330	1. PCB H77-D3H REV1.01 --> H77-D3H-MVP REV1.01	
	2. Add Lucid vertune function	

Circuit or PCB layout change

DATE	Change Item	Reason
P67X-UD3-B3		
2011/02/18-0.1	1. 移除LAR11 ,LAR14 , NR28 ,新增NTP11	
2011/02/18-1.0	2. 新增DR388,DR389,DR391 ; Remove DQ49,DR347,DR371 3. CR44改成R0603-RH 4. R1,LAR3,RBR20,LABC25 -->R0402-2-SHORT 5. RAQ1 --> Q_TO223-MASK 6. RARN1 --> R8P4R-0402-SHORT 7. CESD1-5 --> SSOP5 8. RAQ2,RAEC1一起往下移40mil 9. CESD2文字面要標pin1	
2011/03/8-1.01	1. Add "Dolby" logo	
2011/03/8-1.02	1. UAFB1,UAFB2,UBF1,UBF2 Footprint update 1206-->1812 2. Add "AD1" FOR 5VSB	
Z68XP-D3		
1.0	1. update MINI_PCIE footprint 2. 文字面 : SLOT部分全對齊	
Z77-D3H-0.1	EVT	
0.2-1216	1. Remove SE9172 , Add VCC8 內層(注意其他內層power,跨切割) 2. SPDIF AGND --> GND 3. PCI SLOT & PCIEX1/X4 CAP COST DOWN 4. 0 ohm --> SHORT PAD 5. REMOVE SMBUS FROM COMP TO SOLDER SIDE IN DR POWER 6. SATA3 connect Change to 90 degree (記得SATA3訊號部分要做挖空) 7. Add "108dB"文字面 8. Remove VCC1_05_PCH & VCC1_8_PCH gate net 9. Add EJ168 R_USB30_1 & F_USB3 10. UAE1/UAE2 NET SWAP 11. 內層+12V要打VIA在COMA處 12. SPDIFO_HDMI走12mil	
1.0	1. SATA2~SATA3文字面要隱藏 2. DART2 移至 DC_DQ1左上方 3. Q7 & DAR31 NET Change	
1.01	1. 0 OHM SHORT PAD (LAN & AUDIO) 2. DDR3 2400MHz OC modify	

BLOCK DIAGRAM



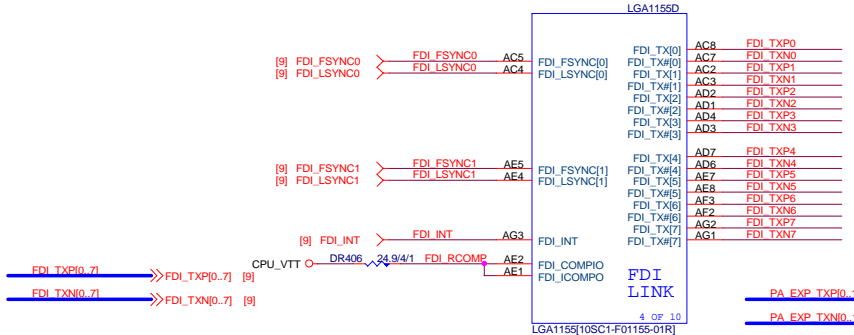
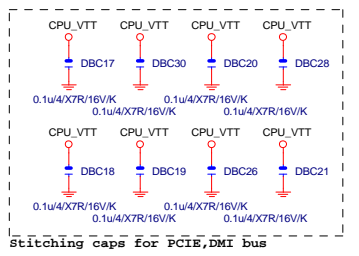
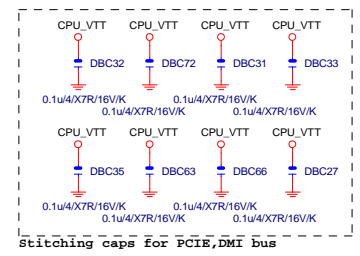
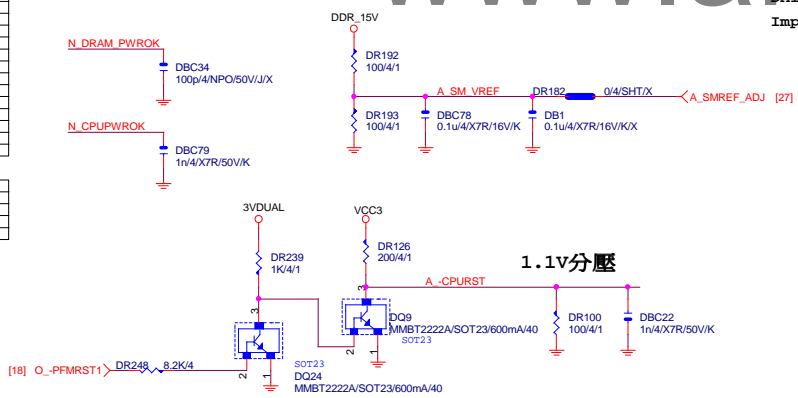


CFG5=1: 1X16 PEG
CFG5=0: 2X8 PEG

CFG	R	L	NOTE
0	RSVD	RSVD	RSVD
1	RSVD	RSVD	RSVD
2	RSVD	RSVD	RSVD
3	RSVD	RSVD	RSVD
4	RSVD	RSVD	RSVD
7	RSVD	RSVD	RSVD
8	RSVD	RSVD	RSVD
9	RSVD	RSVD	RSVD
10	RSVD	RSVD	RSVD
11	RSVD	RSVD	RSVD
12	RSVD	RSVD	RSVD
13	RSVD	RSVD	RSVD
14	RSVD	RSVD	RSVD
15	RSVD	RSVD	RSVD
16	RSVD	RSVD	RSVD
17	RSVD	RSVD	RSVD

CFG6	CFG5	PCIE CONFIG
1	1	1X16 , Default
1	0	2X8
0	1	RSVD
0	0	X8 ,X4 ,X4

CFG 0-17 all internal PULL-UP

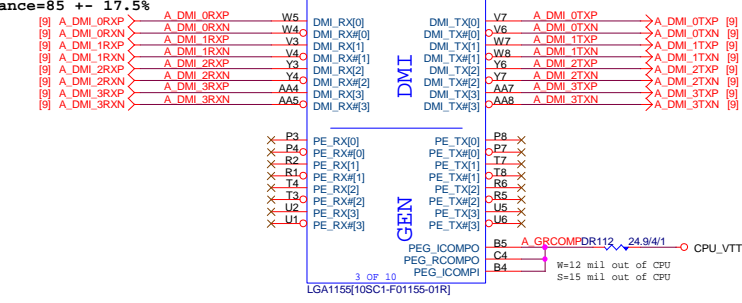


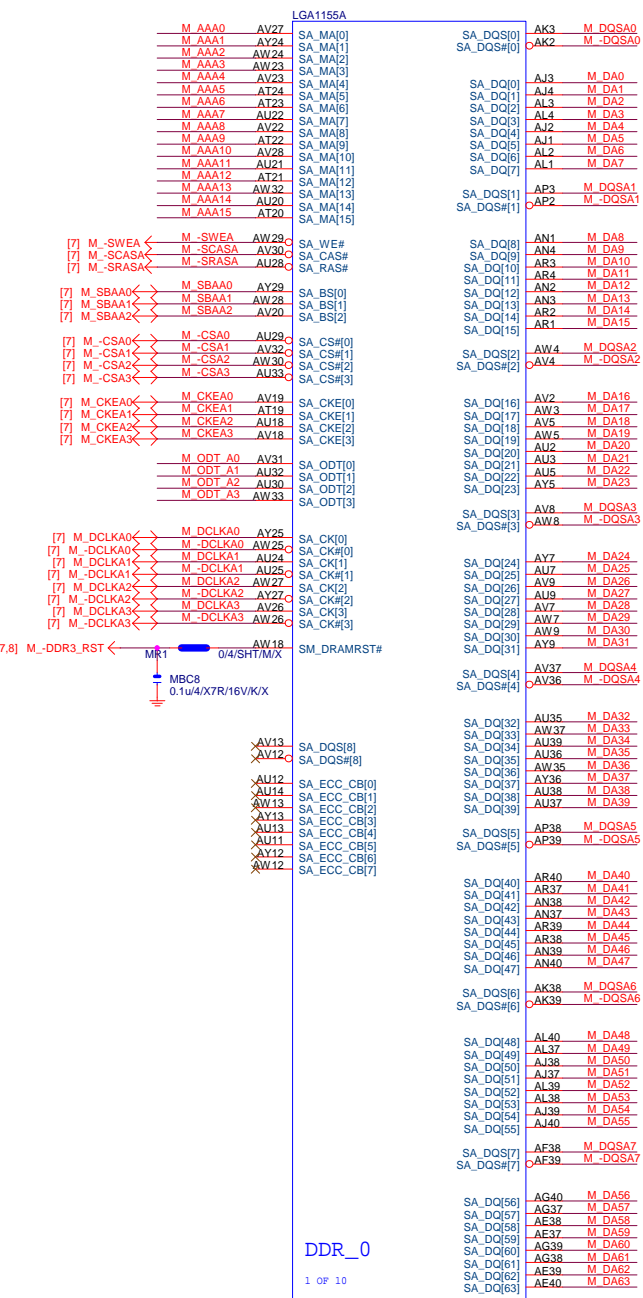
FDI:12/4/5/4/12
Impedance=85 +- 17.5%

PCIEX16:16/5/5/5/16(breakout min 10/4/4/4/10)
Impedance=80 +- 17.5%

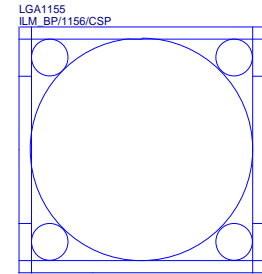
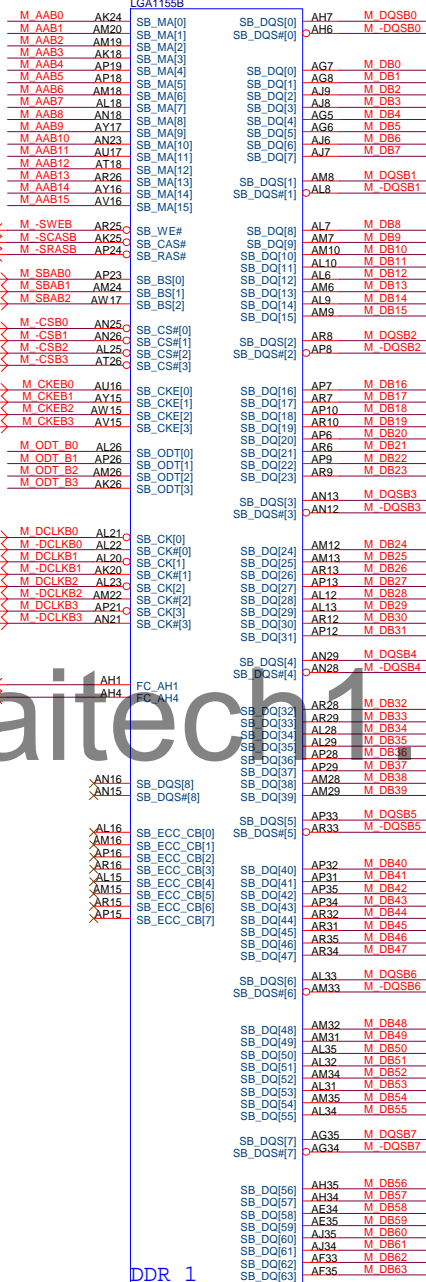


DMI:12/4/5/4/12
Impedance=85 +- 17.5%

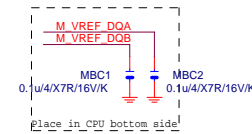


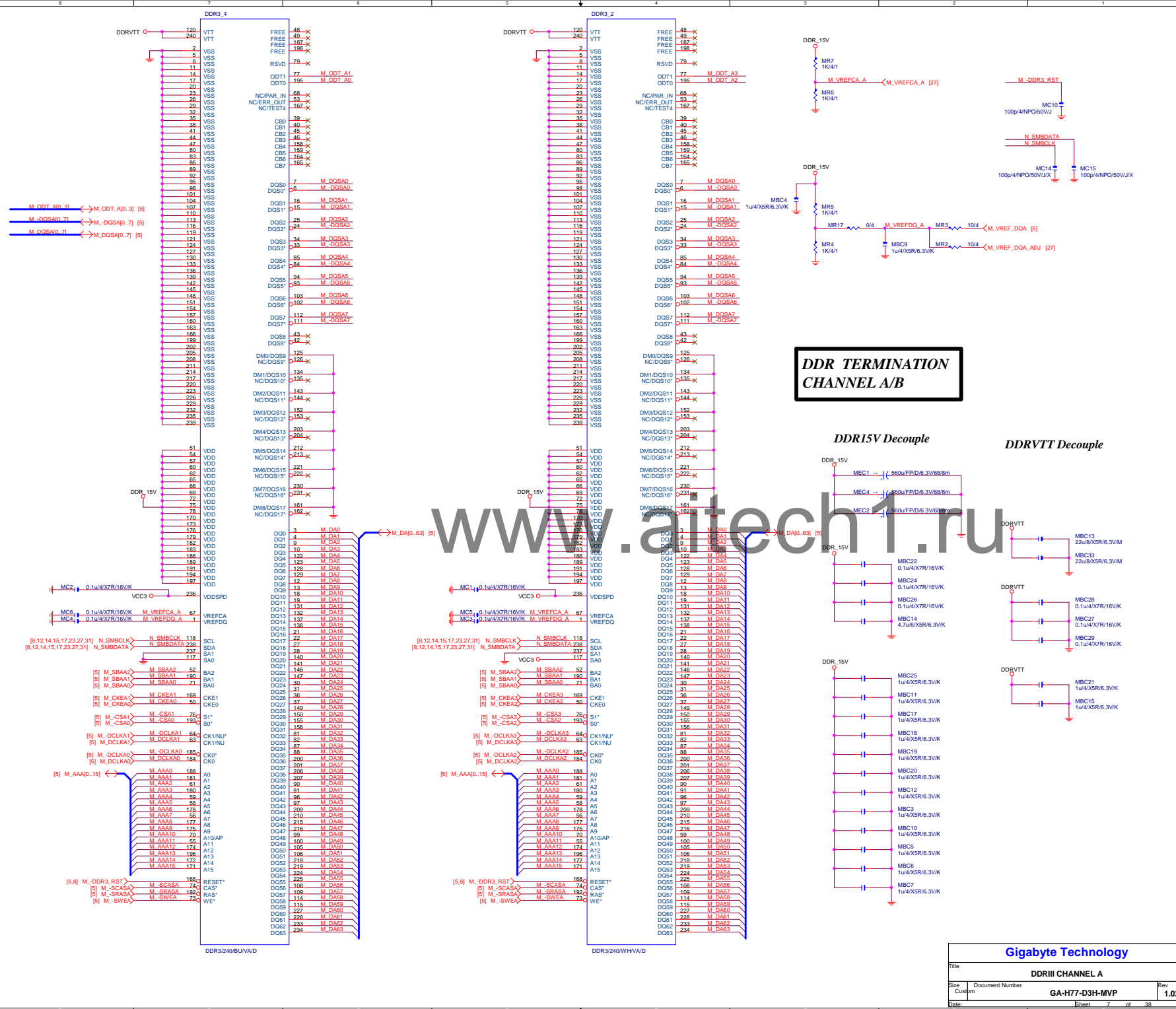


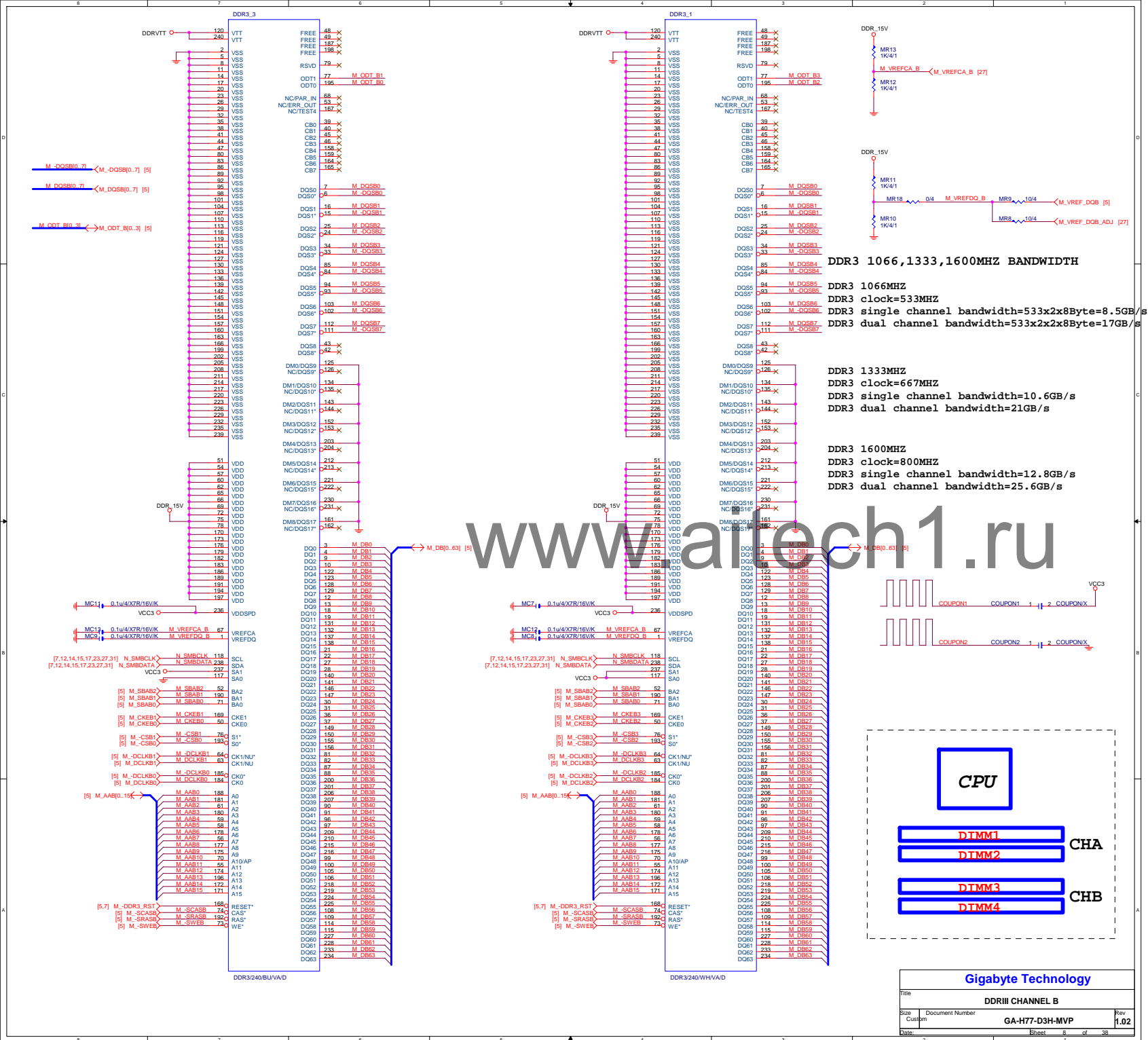
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Need check the new CPU ME







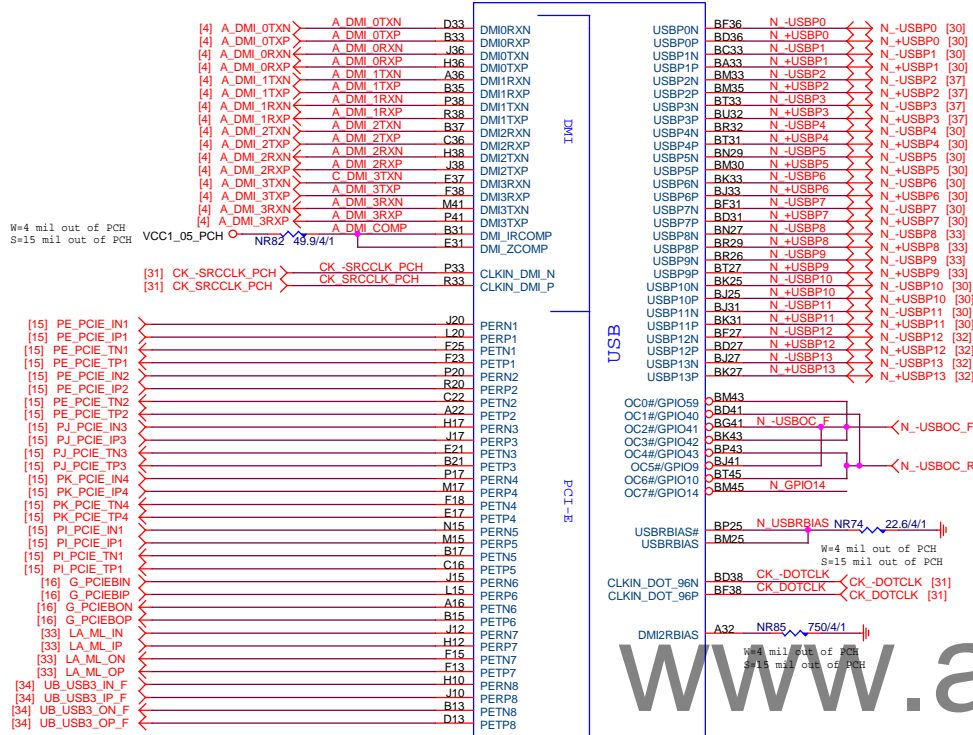
USB3.0:20/5/7/5/20 (breakout min 8/4/4/4/8) ; ONLY 3 VIAS
Impedance=85 +- 17.5%
Back Panel < 10000 MILS
Front Panel < 6000 MILS

USB2.0 : 12/4.5/7.5/4.5/12 (breakout min 8/4/4/4/8)
Impedance=90 +- 17.5%

PCBH

PCHG

FDILINK



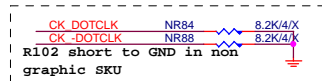
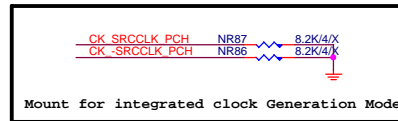
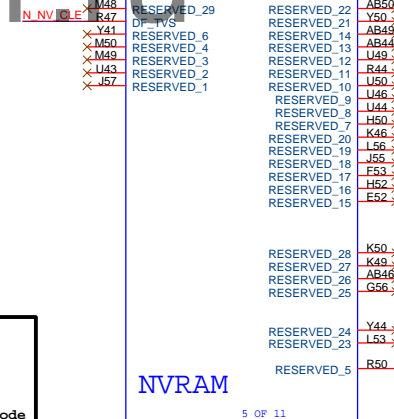
OC[3:0]# for Device 29 (ports 0-7)
OC[7:4]# for Device 26 (ports 8-13)

USB OC# Configure	
OC0#	USB0,1
OC1#	USB2,3
OC2#	USB4,5
OC3#	USB6,7
OC4#	USB8,9
OC5#	USB10,11
OC6#	USB12,13
OC7#	Not Use

FDI_TXP0_7I >>> FDI_TXP0[0..7] [4]
FDI_TXN0_7I >>> FDI_TXN0[0..7] [4]

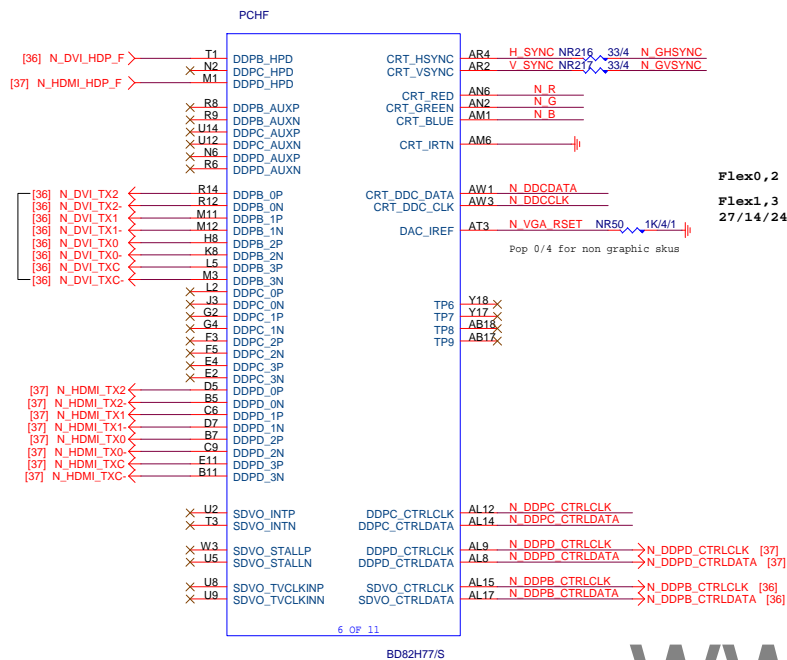
FDI:12/4/5/4/12
Impedance=85 +- 17.5%

PCHE

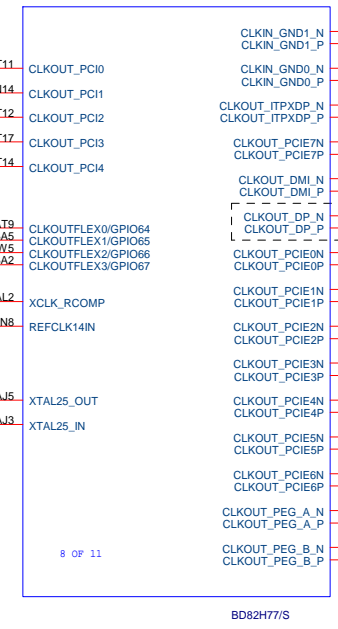
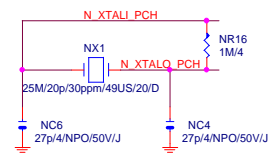


Gigabyte Technology

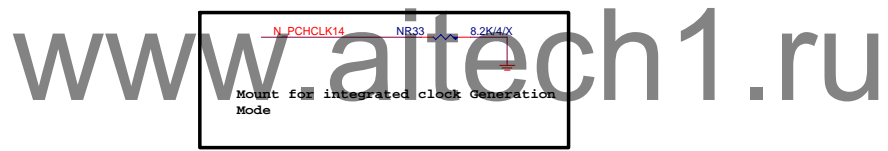
Title			
PCH FDI,DMI,USB,PCI-E			
Size	Document Number	Rev	1.02
Custom	GA-H77-23H-MVP		
Date:	Friday, April 06, 2012	Sheet	9 of 38



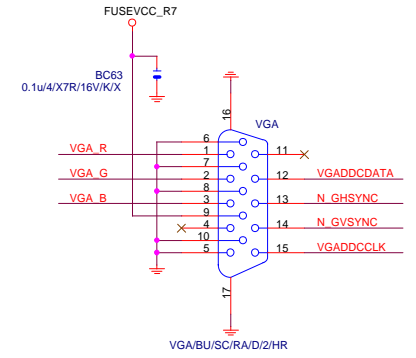
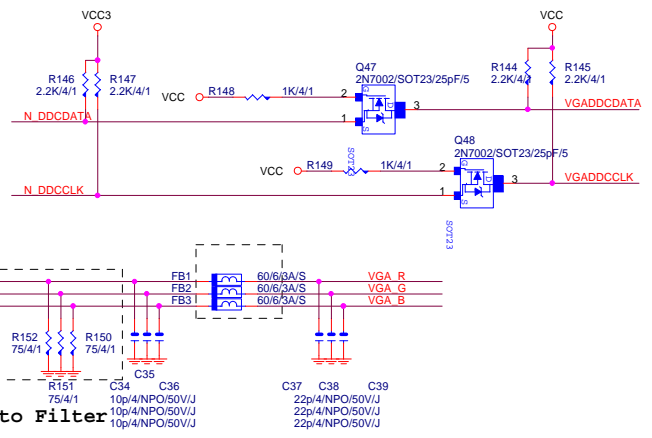
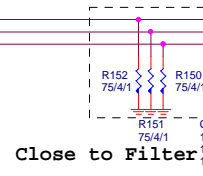
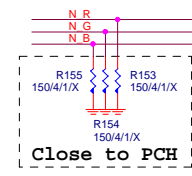
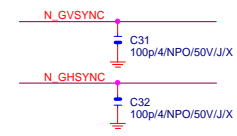
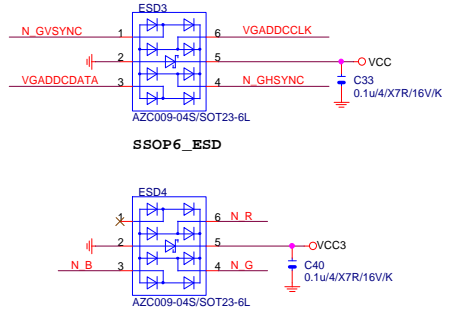
Flex0,2 : 33MHZ
Flex1,3 :
27/14/24/48/25MHZ



Differential Clock:18/4/6/4/18
Impedance=90 +- 15%

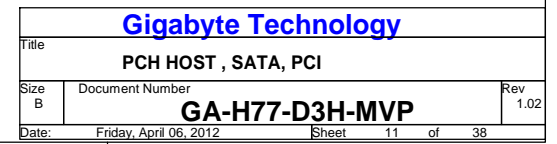


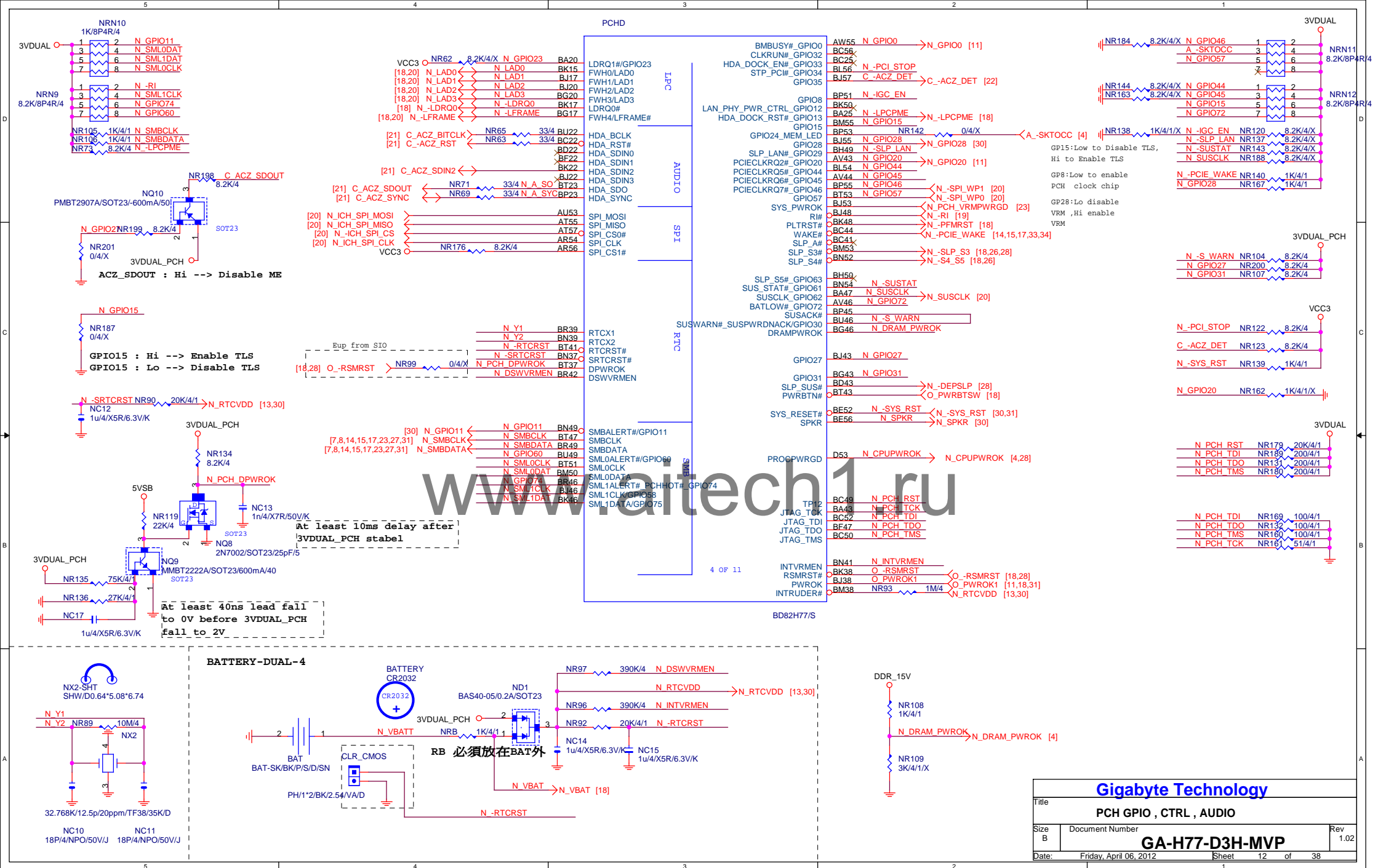
Check if NC for P67 non graphic chip

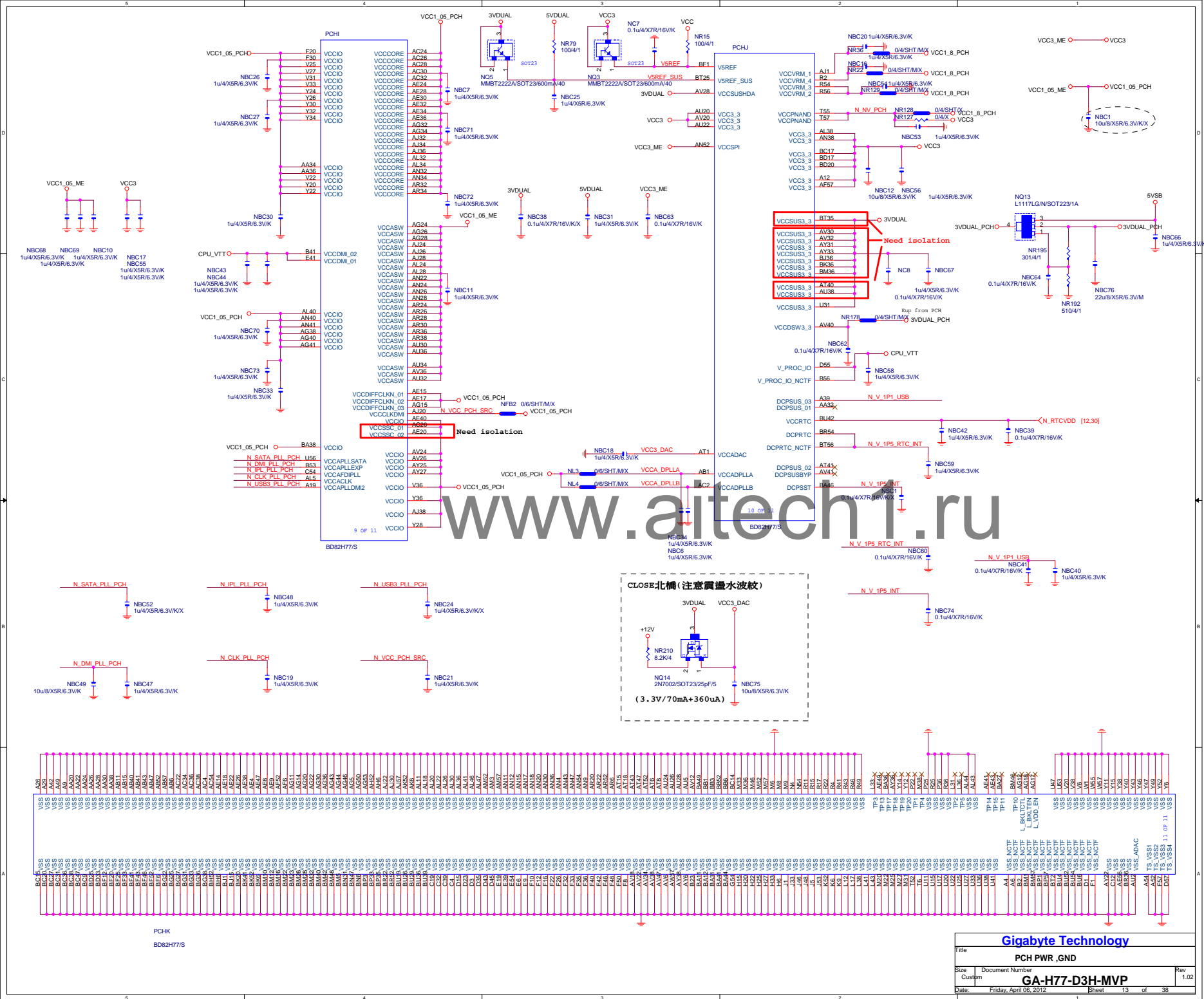


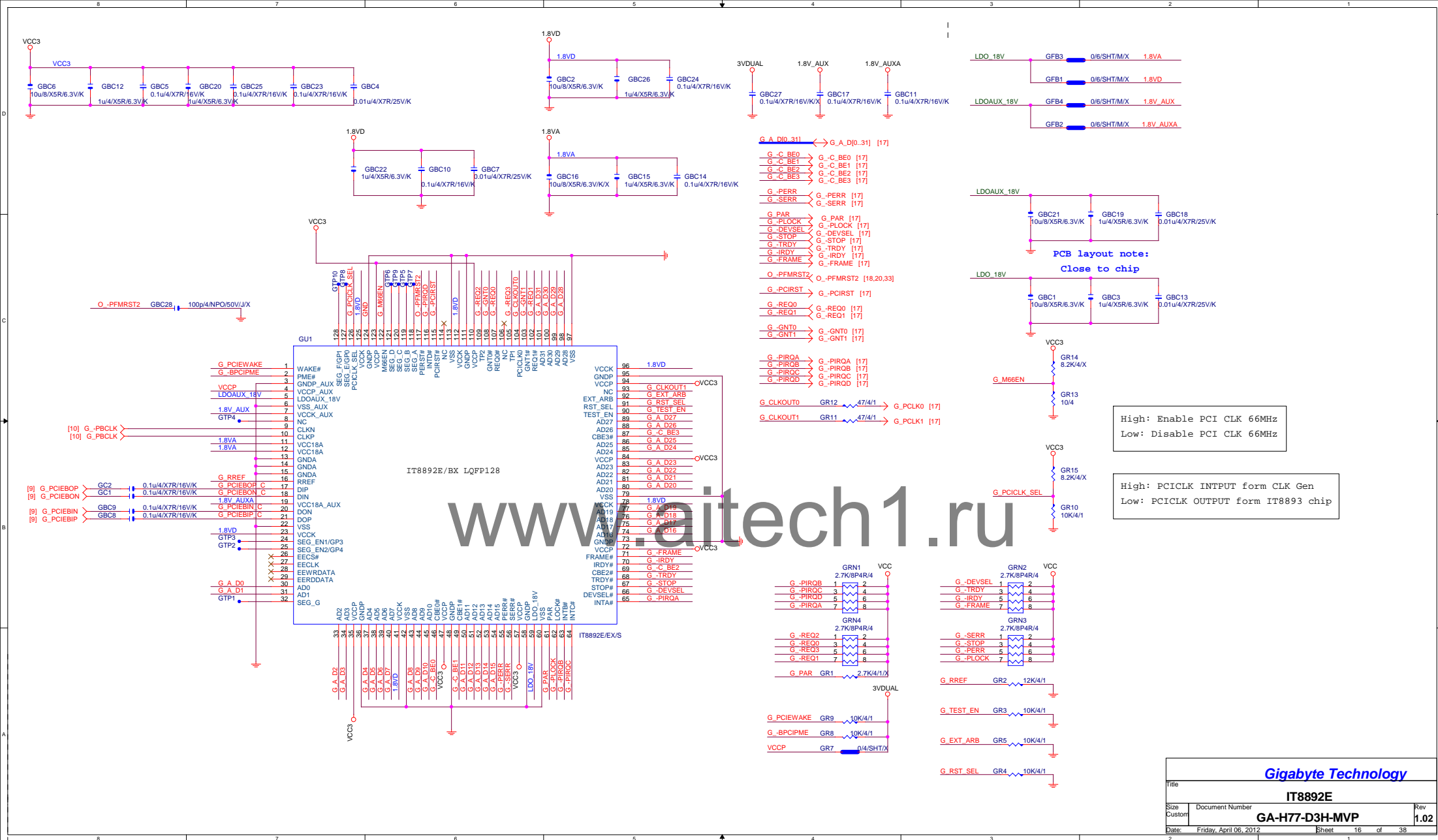
Gigabyte Technology				
Title PCH DISPLAY ,CLK BUFFER				
Size Custom	Document Number GA-H77-D3H-MVP			Rev 1.02
Date:	Friday, April 06, 2012	Sheet	10	of 38

SATA2 : 15/7.5/4.5/7.5/15 (breakout min 8/4/4/4/8)
Impedance=90 +- 17.5%

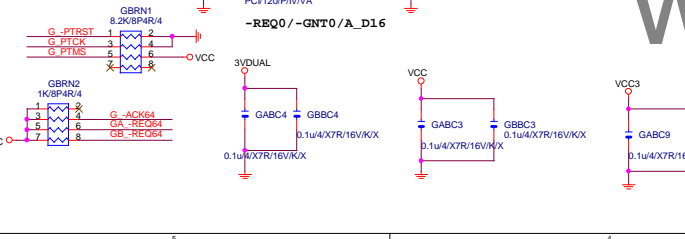
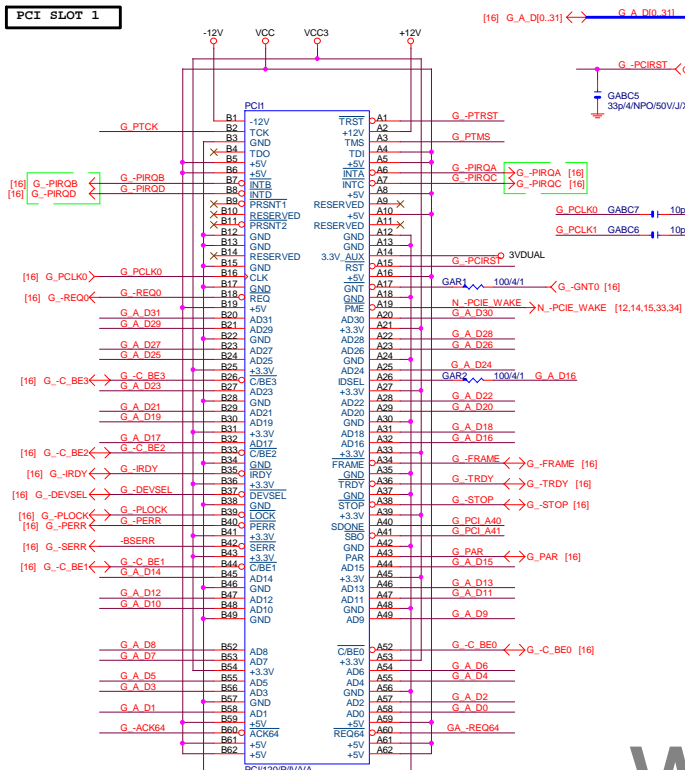




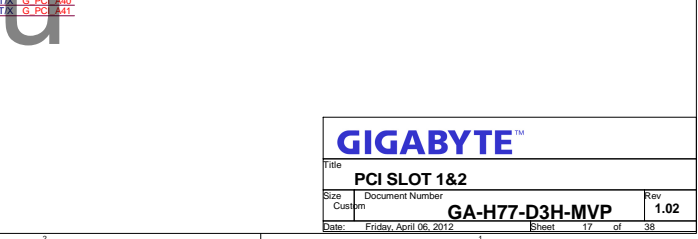
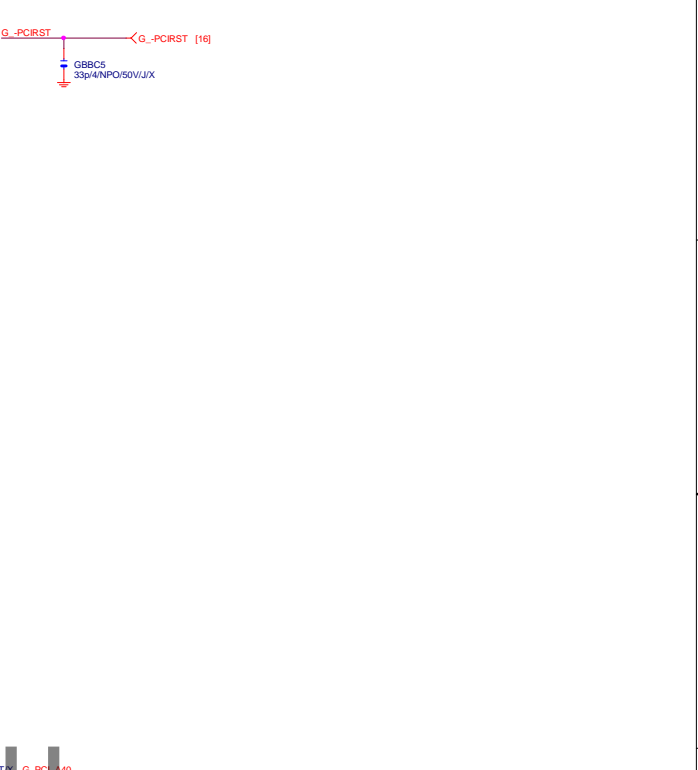
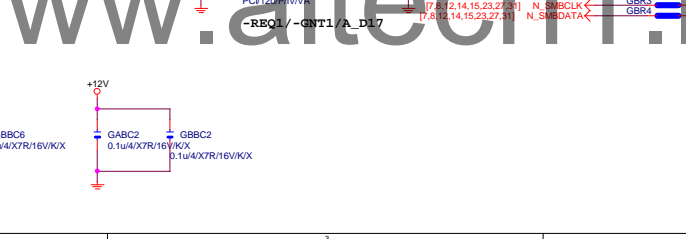
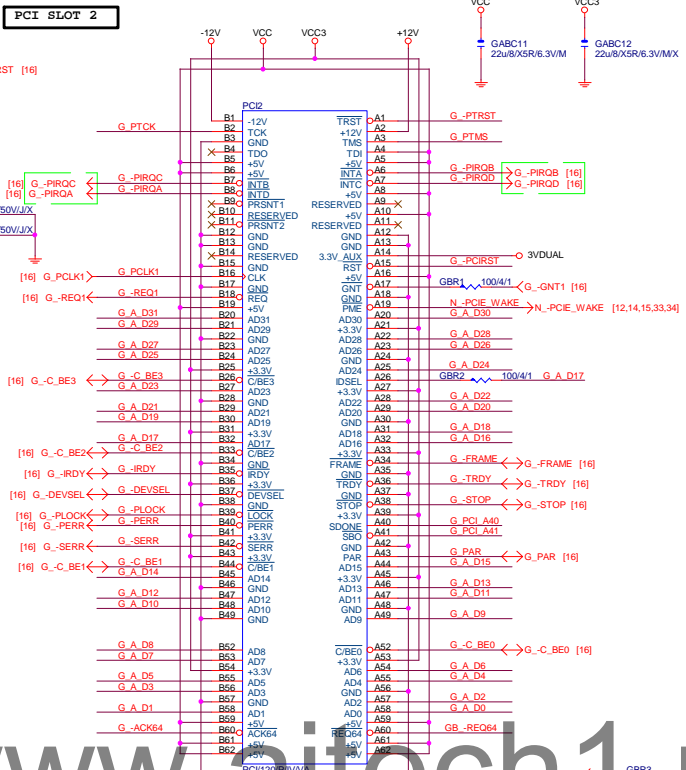




PCI SLOT 1

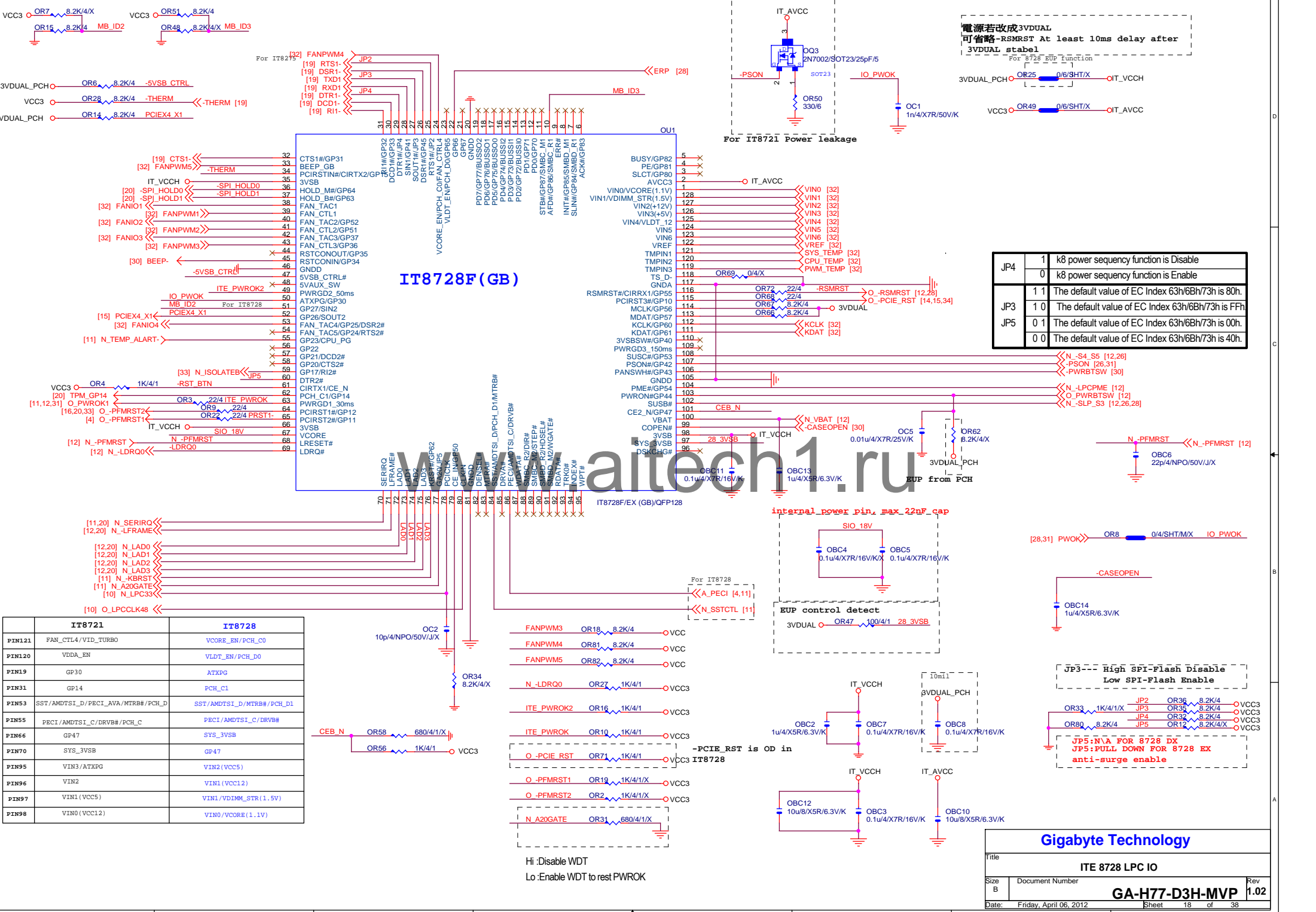


PCI SLOT 2



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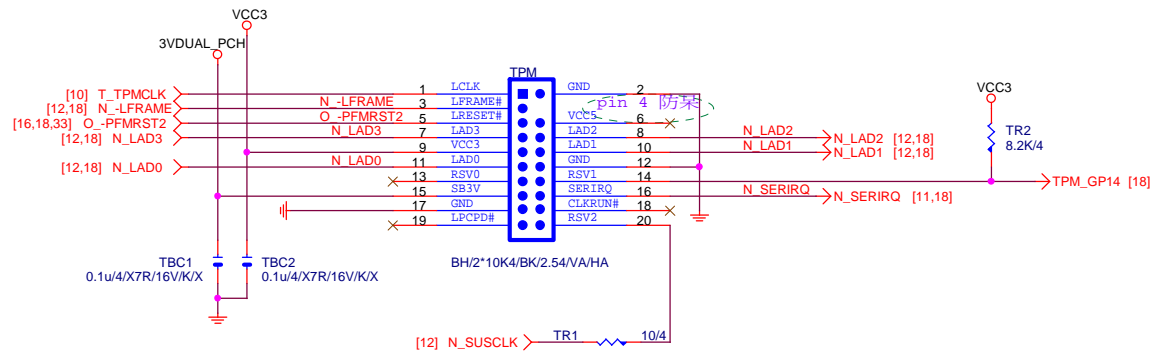
GIGABYTE™			
PCI SLOT 1&2			
Size	Document Number	Rev	
Custom	GA-H77-D3H-MVP	1.02	
Date:	Friday, April 06, 2012	Sheet	17 of 38



電源若改成3VDUAL
可省略-RSMRST At least 10ms delay after
3VDUAL stabel

JP4	1	k8 power sequency function is Disable
	0	k8 power sequency function is Enable
JP3	1 1	The default value of EC Index 63h/6Bh/73h is 80h.
	1 0	The default value of EC Index 63h/6Bh/73h is FFh
JP5	0 1	The default value of EC Index 63h/6Bh/73h is 00h.
	0 0	The default value of EC Index 63h/6Bh/73h is 40h.

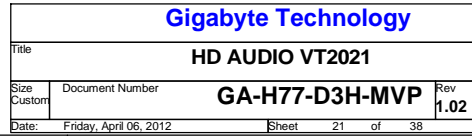
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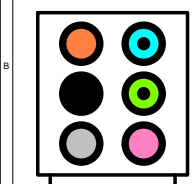
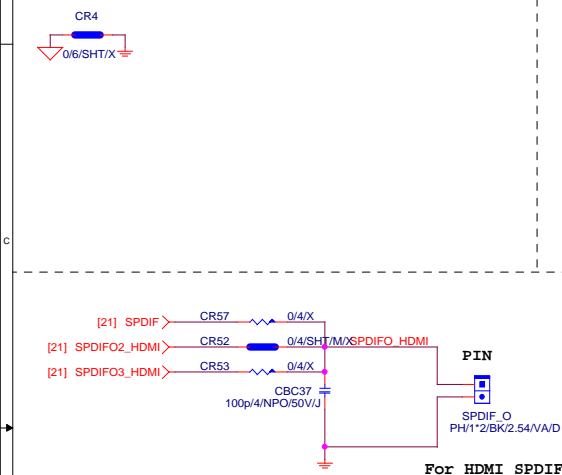


Gigabyte Technology			
Title		BIOS	
Size	Document Number	GA-H77-D3H-MVP	Rev 1.02
Custom			
Date:	Friday, April 06, 2012	Sheet 20 of 38	

CR36: 20K/4/1% @Realtek cdec & VT1708S-CE
CR36: 5.1K/4/1% @VIA codec VT1708S-CD/VT2021
CBC38 100p @VIA codec VT1708S

The diagram shows a circuit with a 100pF capacitor (CBC38) connected to a 5.1K resistor (CR36) in series with a 20K resistor (CR36). The output is connected to a 50V/0.5V/JX source.





AZALIA JACK

AUDIOB

BLUE
LINE-IN

GREEN
LINE-OUT

PINK
MIC-IN

AUDIOA

Orange
CEN/LFE

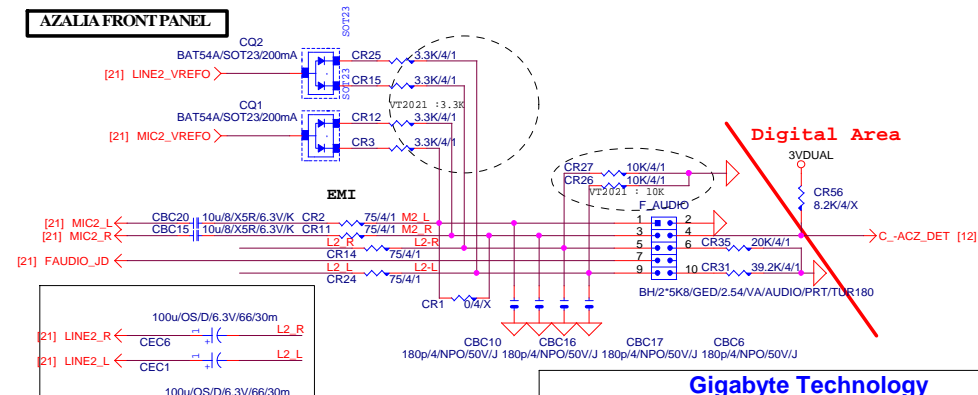
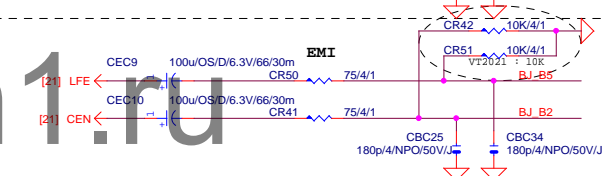
Black
SURROUND

SPDIF

OPTICAL

2X3RP/25P/BU,GE,OR,BK,GY,RA[11NR6-403025-61R]

2X3RP/25P/BU,GE,OR,BK,GY,RA[11NR6-403025-61R]

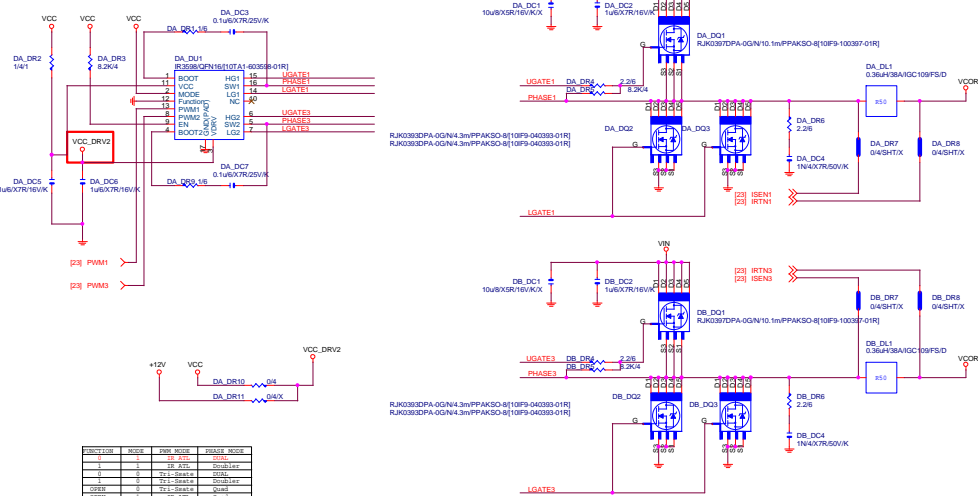


3VDUAL
CR56
8.2K/4X

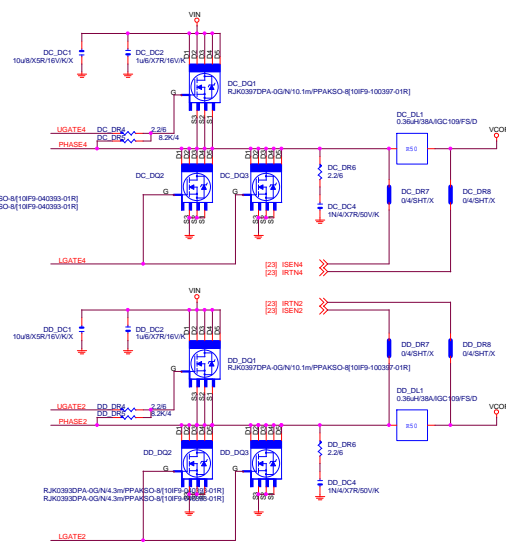
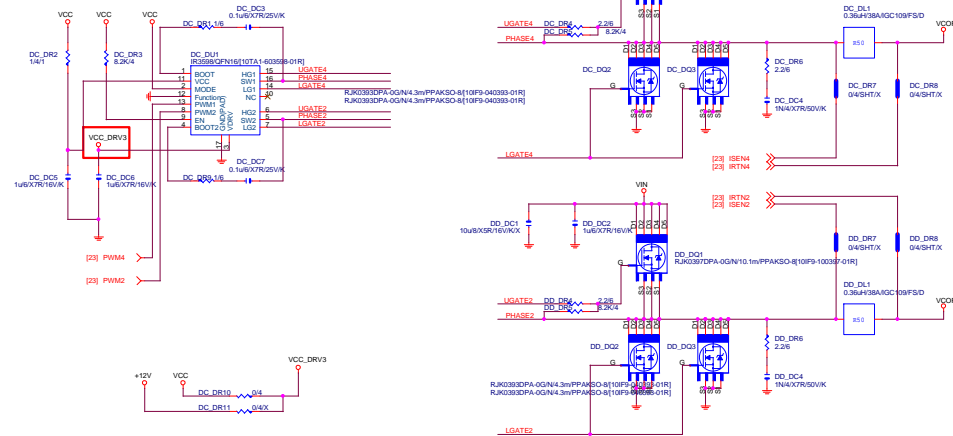
2
4
6 CR35 20K/4/1
10 CR31 39.2K/4/1
5K8/GED/2.54/VA/AUDIO/PRT/TUR180
C_-ACZ_DET [12]

Title				AUDIO JACK			
Size Custom		Document Number				Rev	
		GA-H77-D3H-MVP				1.02	
Date: Friday, April 06, 2012				Sheet 22 of 38			

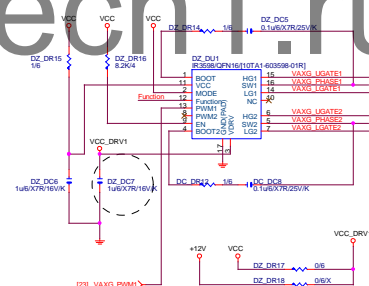
VCORE Phase 1,3



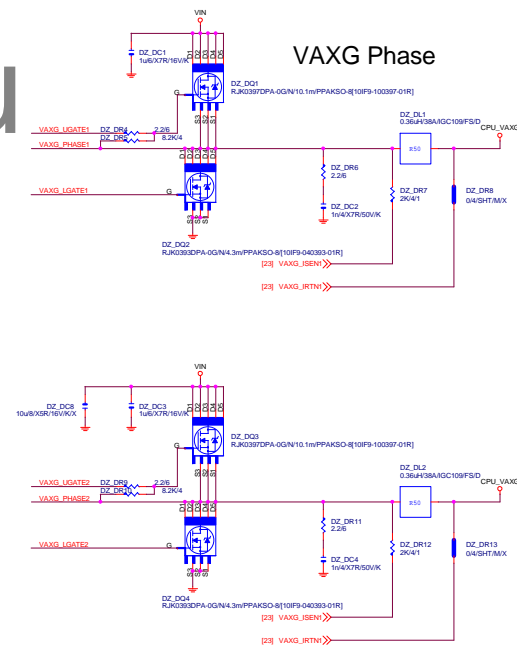
VCORE Phase 4,2



VAXG PHASE 1,2



VAXG Phase

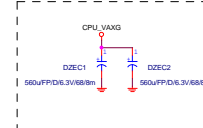


MOS HEATSINK

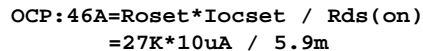


PHASE	MODE	PHASE	MODE
1	1E 3T	1E 3T	1E 3T
2	1E 3T	1E 3T	1E 3T
3	1E 3T	1E 3T	1E 3T
4	1E 3T	1E 3T	1E 3T
5	1E 3T	1E 3T	1E 3T
6	1E 3T	1E 3T	1E 3T
7	1E 3T	1E 3T	1E 3T
8	1E 3T	1E 3T	1E 3T
9	1E 3T	1E 3T	1E 3T
10	1E 3T	1E 3T	1E 3T

In Quad mode, I2C pin10 link to I2C pin10
I2C pin10 link to I2C pin10 without R2



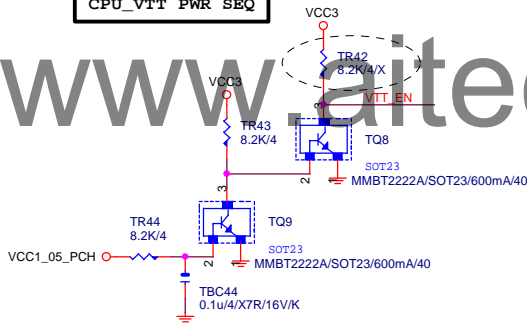
CPU_VTT



CPU_VTT PWR SEQ

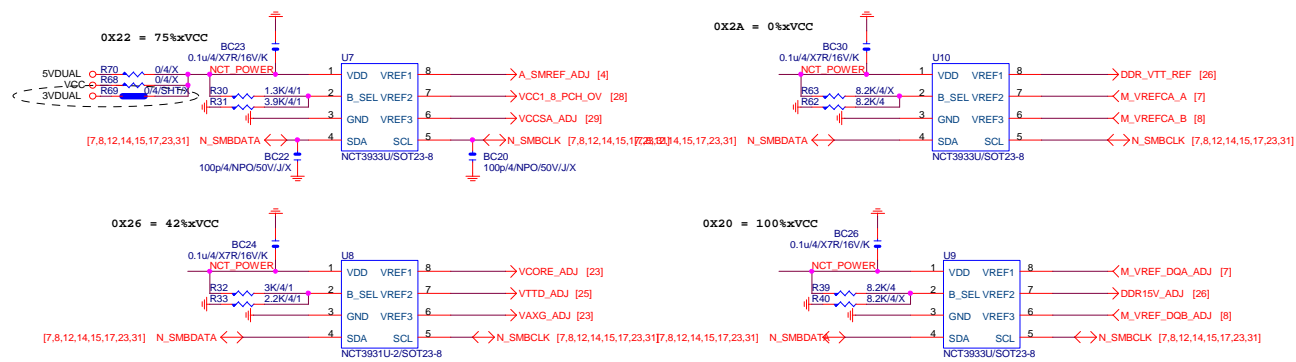
	VTT_SEL
HI	1.05V
LO	1.0V

According intel
CDI/IBP#476733, 固定1.05V



GIGABYTE™

Title			
RT8120_CPU_VTT			
Size	Document Number	Rev	
Custom	GA-H77-D3H-MVP	1.02	
Date:	Friday, April 06, 2012	Sheet	25 of 38



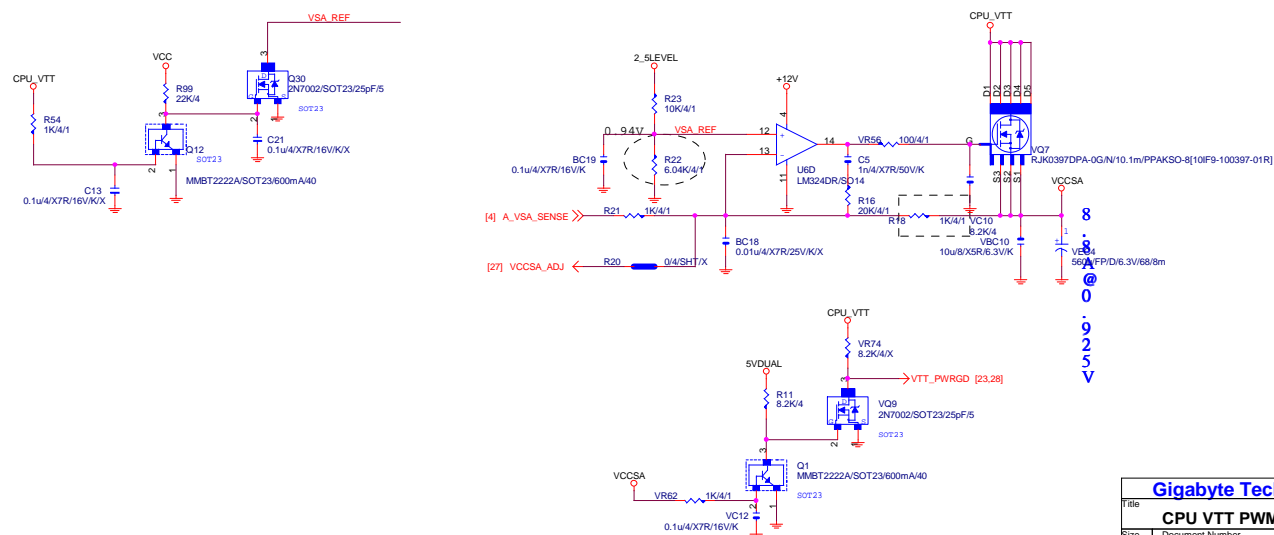
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VREF2	VREF_DDRA_CA	DDR15V	VCC1_8_PCH	CPU_VTT
VREF3	VREF_DDRA_CA	VREF_DDRB_DQ	VCCSA	VAXG

Gigabyte Technology			
Title		CPU CORE VR-2	
Size	Document Number	GA-H77-D3H-MVP	Rev 1.02
Date	Friday, April 06, 2012	Sheet 27	of 38

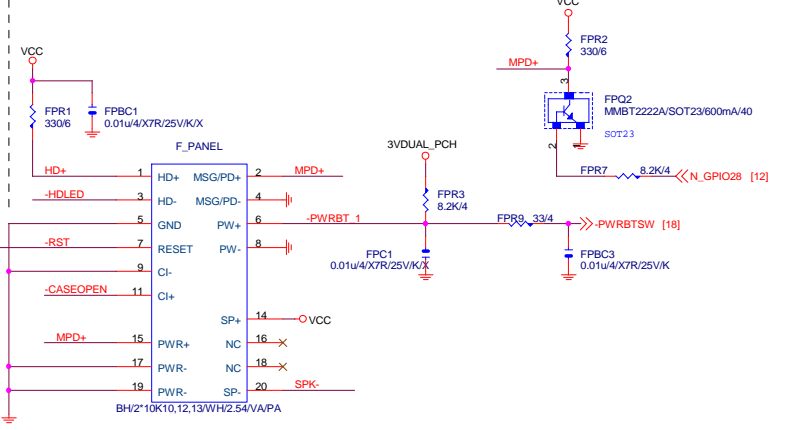
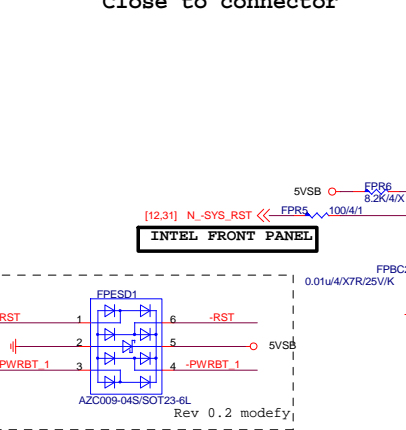
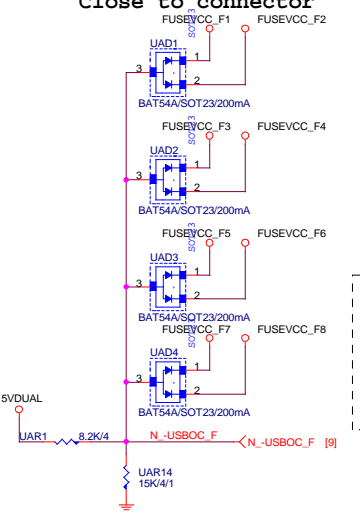
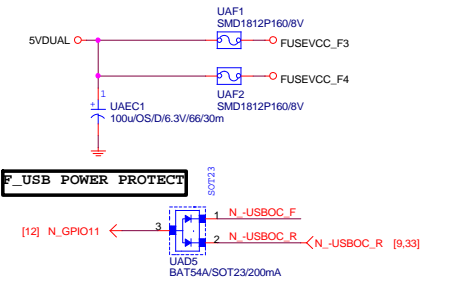
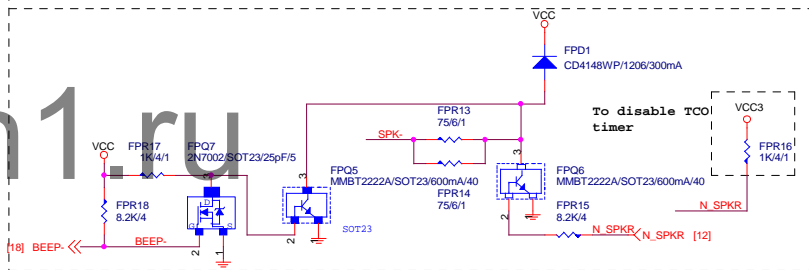
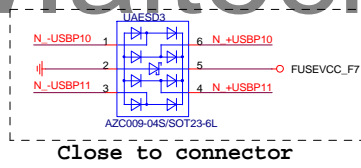
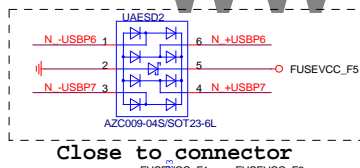
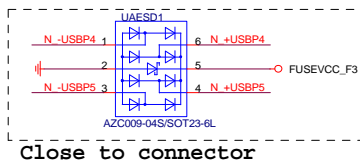
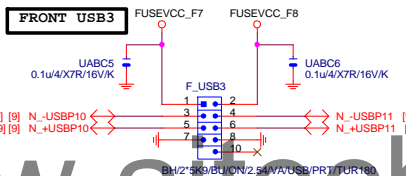
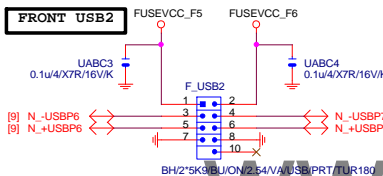
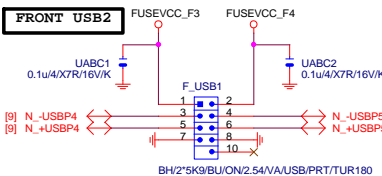
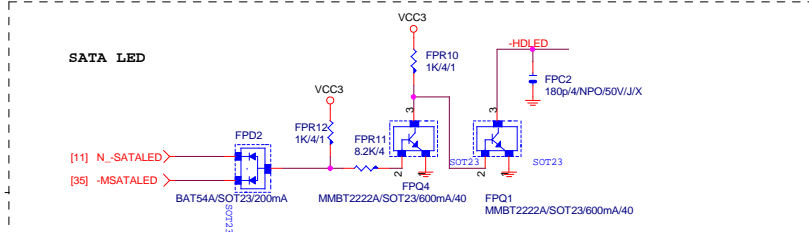
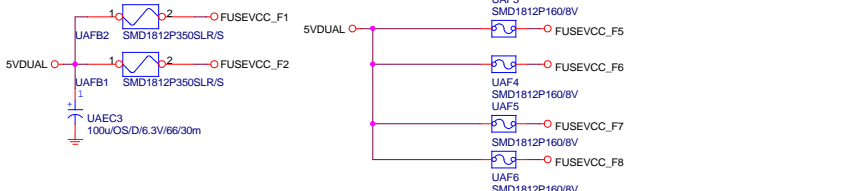
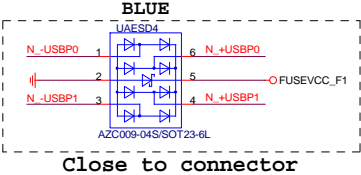
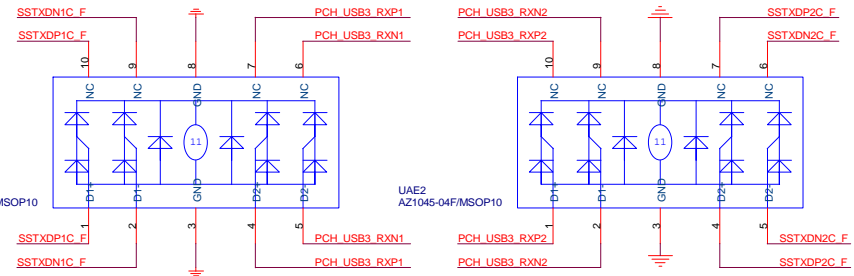
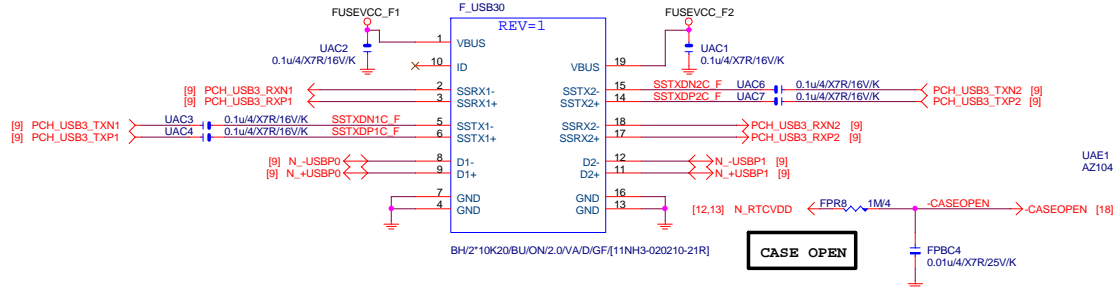
www.aitech1.ru

VCC_SA

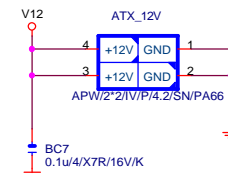
www.aitech1.ru



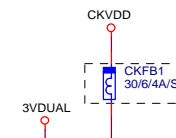
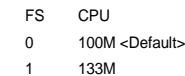
Front USB3.0



ATX POWER CONNECTOR



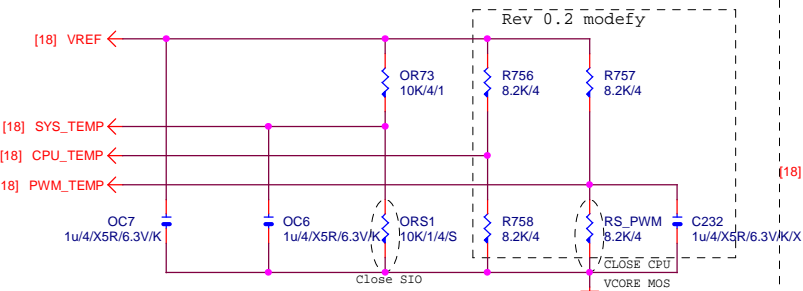
CLK GEN



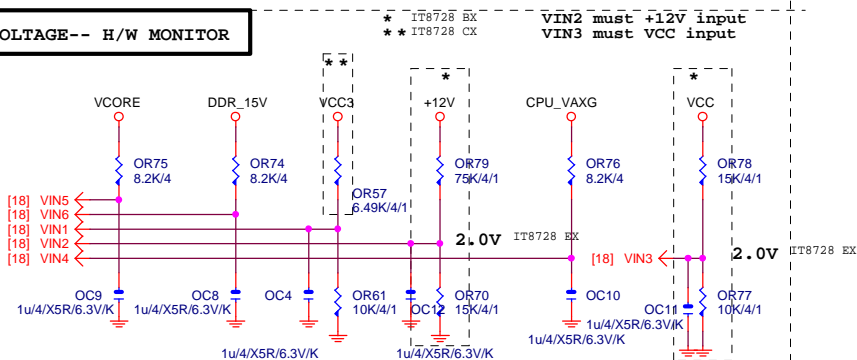
Gigabyte Technology

Title			
ATX POWER CONNECTOR			
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TEMP H/W MONITOR

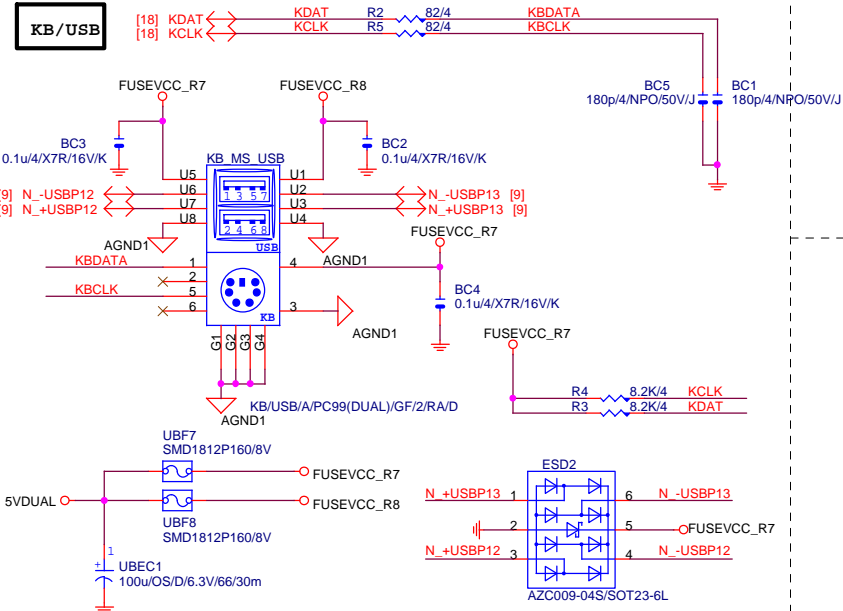


VOLTAGE-- H/W MONITOR

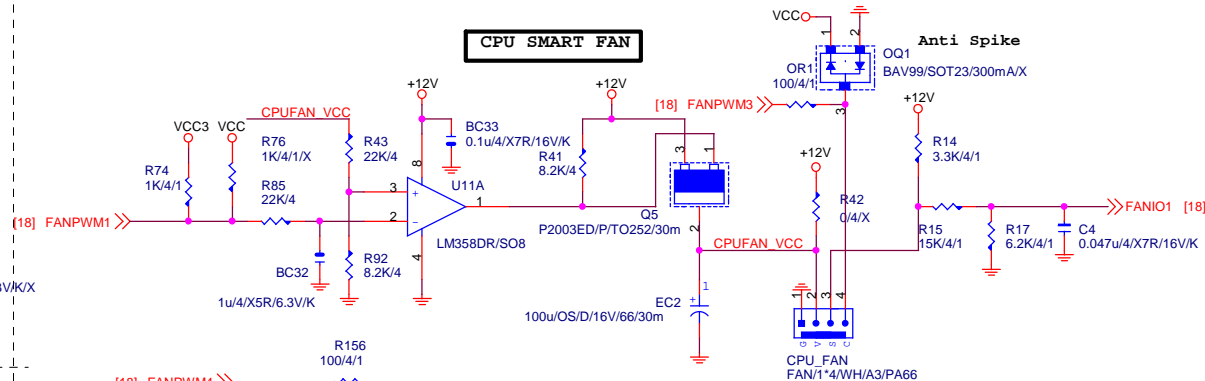


The division voltage of VIN2 & VIN3 must be around 2.9V

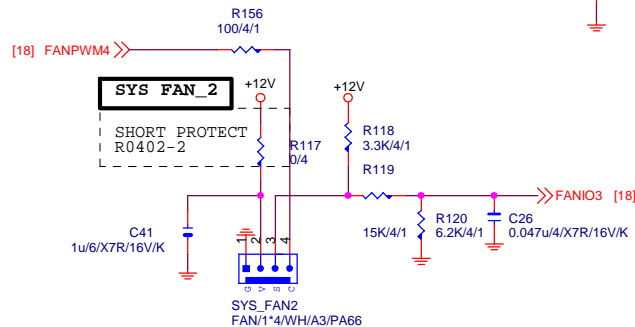
KB/USB



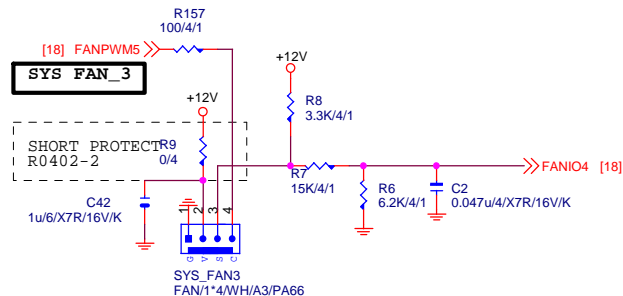
CPU SMART FAN



SYS FAN_2 +12V

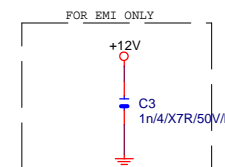
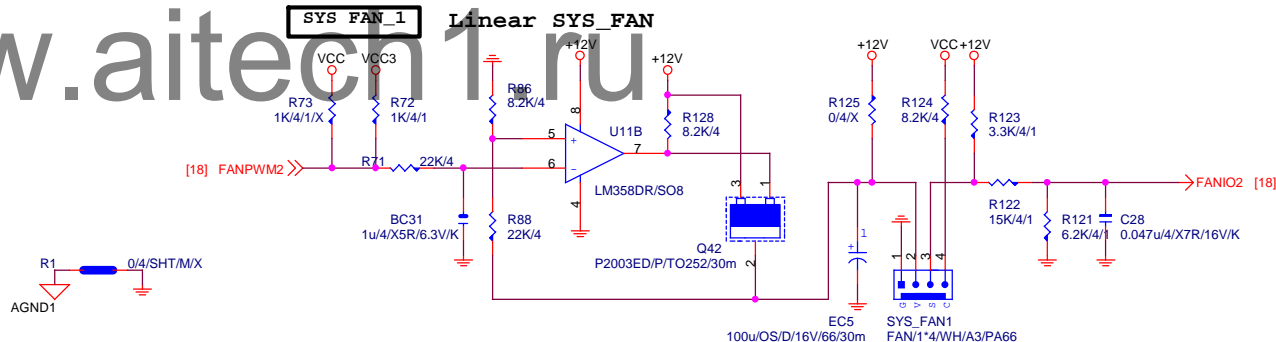


SYS FAN_3



SYS_FAN_1

Linear SYS_FAN



Gigabyte Technology

HWM.KB/MS. FAN CTRL

Size	Document Number
Custom	GA

GA-H77-D3H-MVP

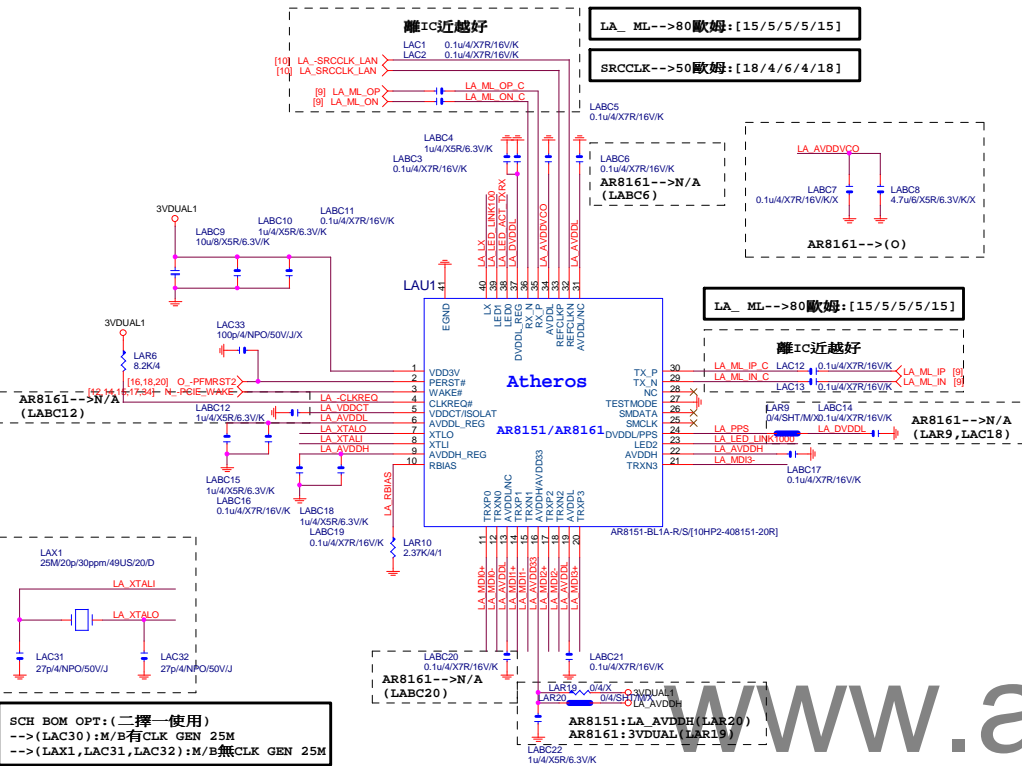
Date: Friday, April 06, 2012

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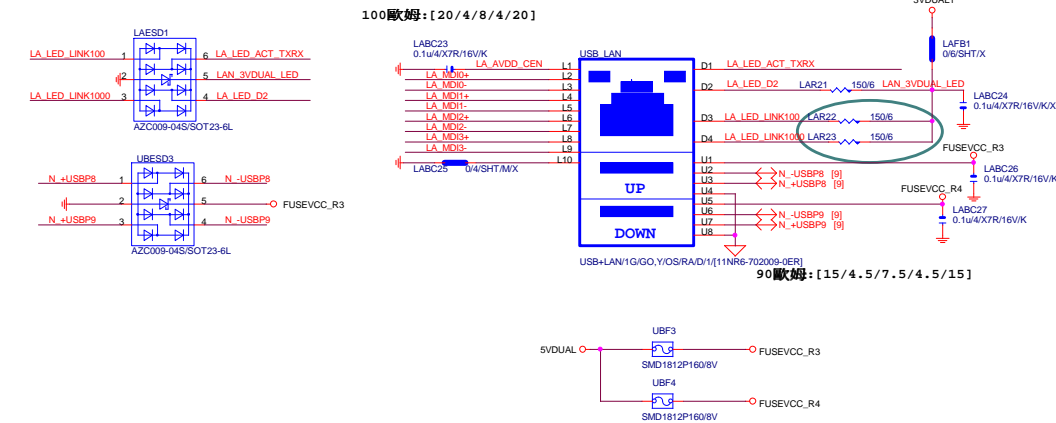
Rev	
1.02	

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LAN:AR8151/AR8161

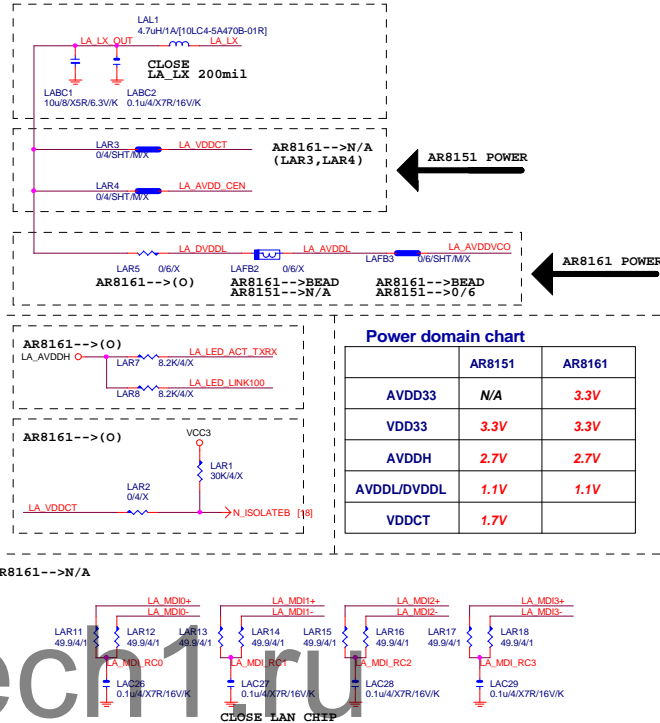


USB30_LAN CONNECTOR



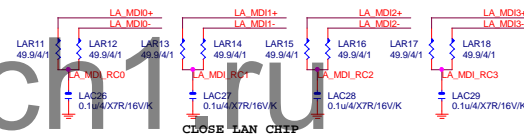
LAN POWER

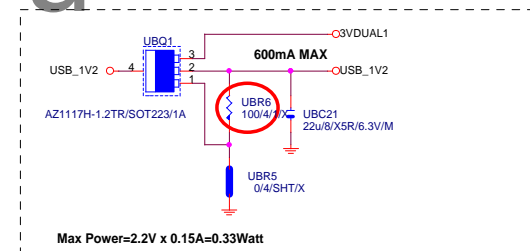
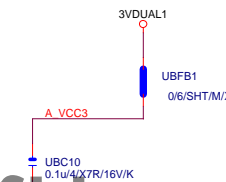
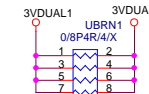
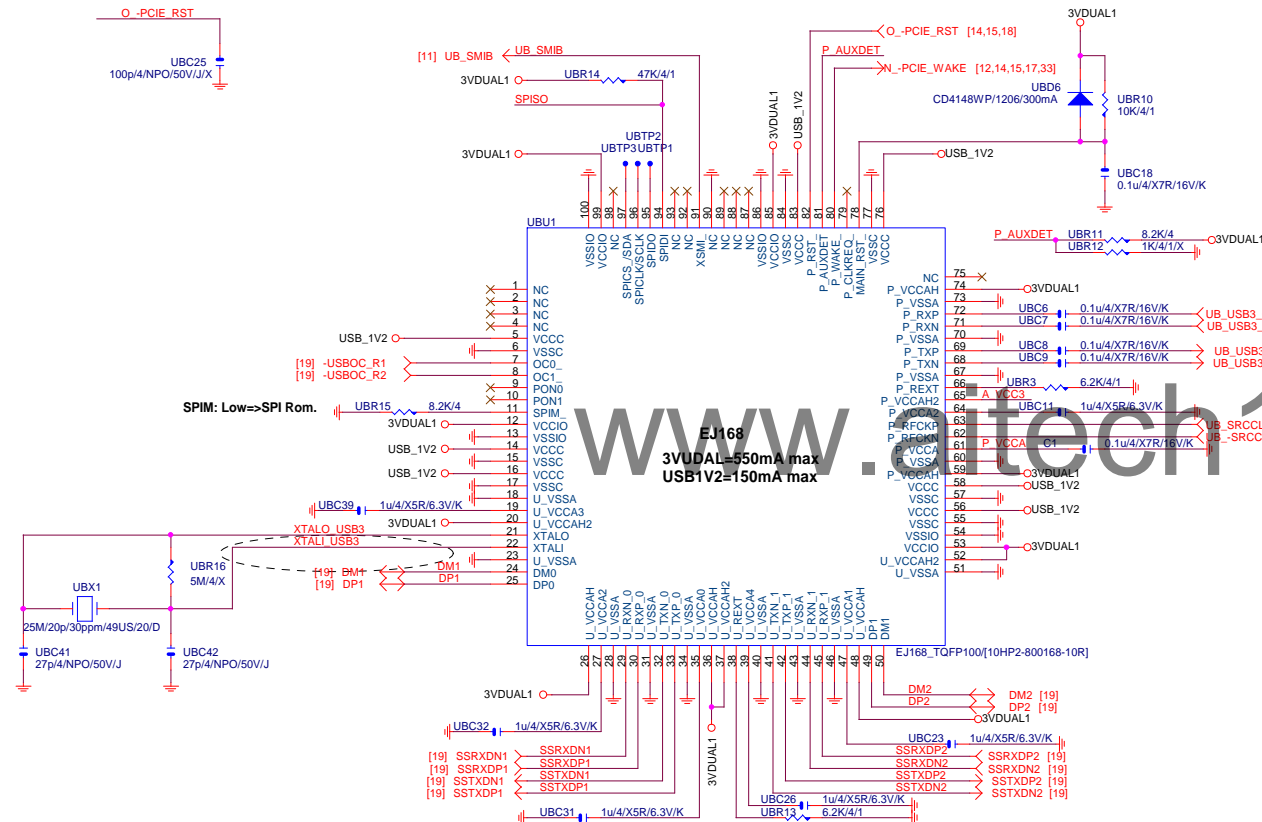
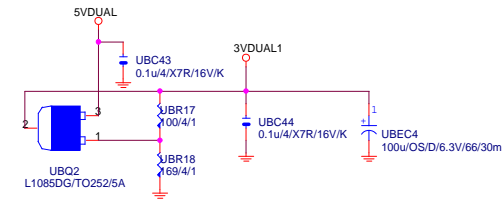
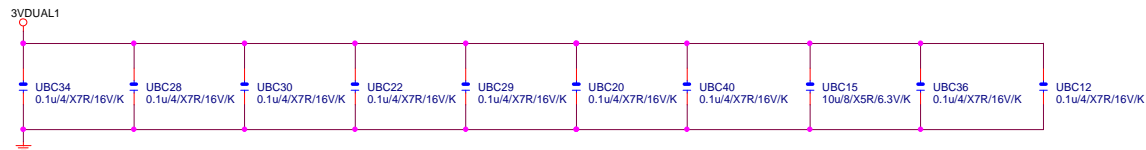
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NEW DESIGN ONLY FOR INTERNAL SWR
AR8151: LAR3(O), LAR5(X)
AR8161: LAR5(O), LAR3/LAR4(X)
```



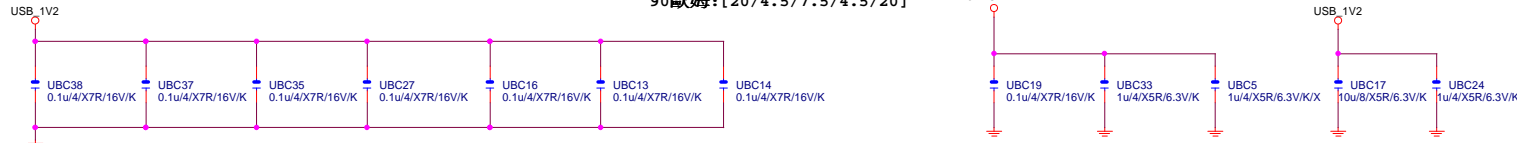
	AR8151	AR8161
AVDD33	N/A	3.3V
VDD33	3.3V	3.3V
AVDDH	2.7V	2.7V
AVDDL/DVDDL	1.1V	1.1V
VDDCT	1.7V	

MDI : AR8161-->N/A



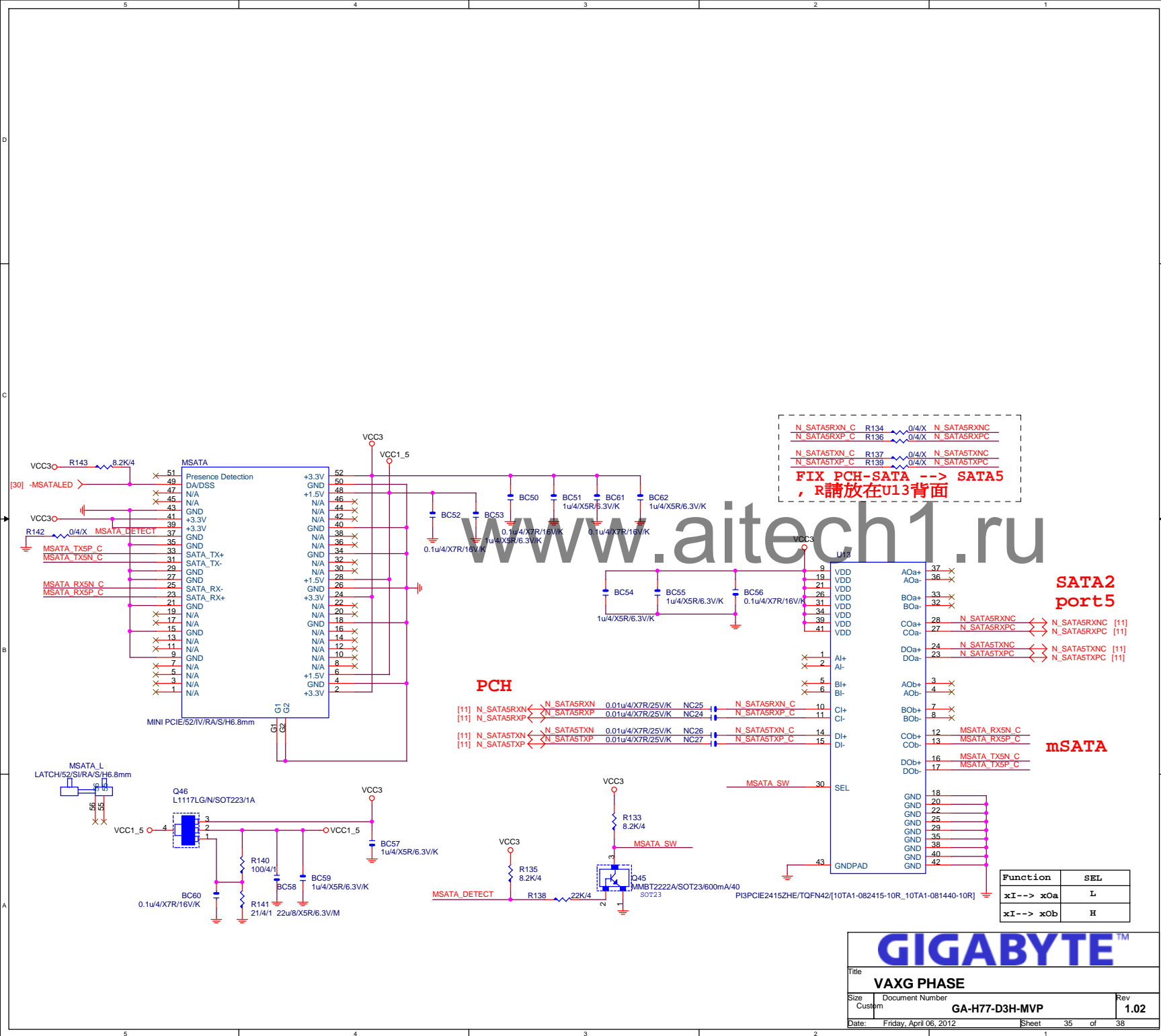


AZ1117H-1.2TR/SOT223/1A-->UR17:0/4,UR16:N/A [1.2V]
L1117LG/N/SOT223/1A-->UR17:0/4,UR16:100/4/1 [1.25V]



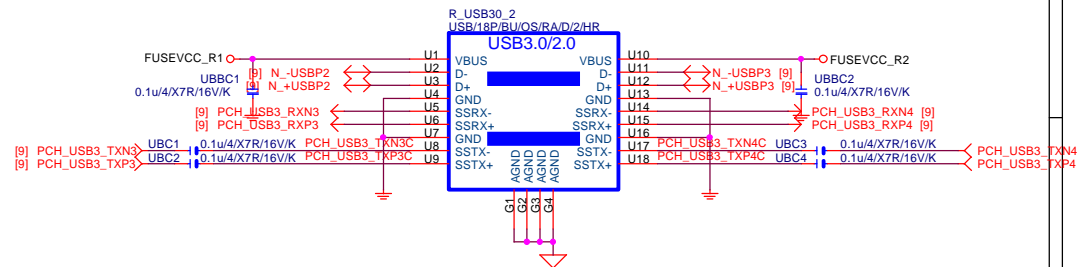
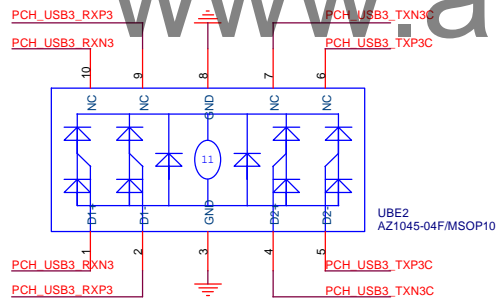
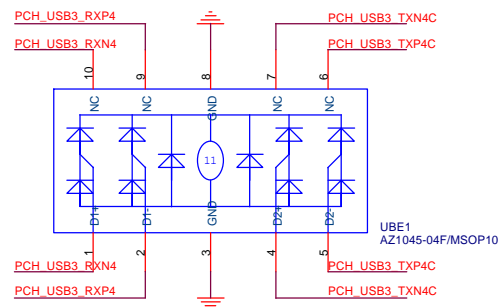
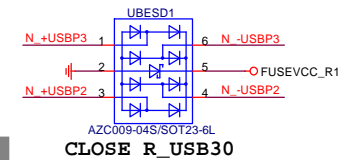
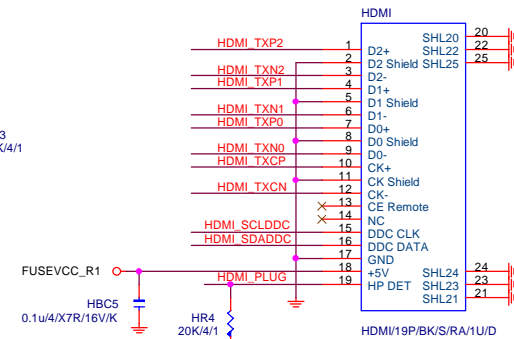
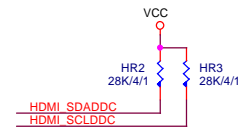
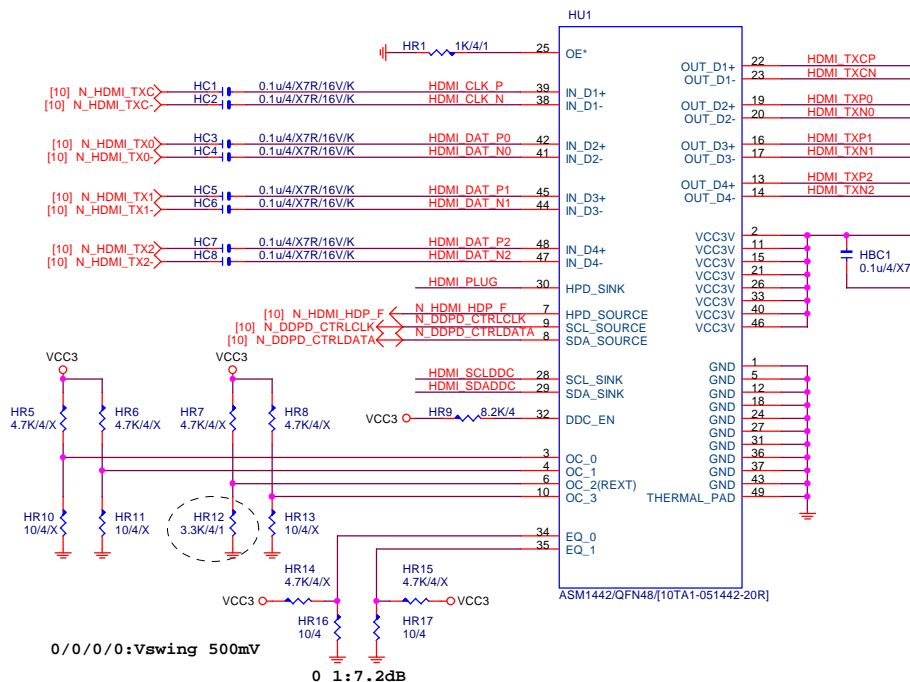
USB3.0 --> 5GHz
BANDWIDTH=5GHz*(8b/10b)=4Gb/s=500MB/s

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Title E-TRON EJ168		
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HDMI:20/4/6/4/20

Impedance=85 +- 17.5%



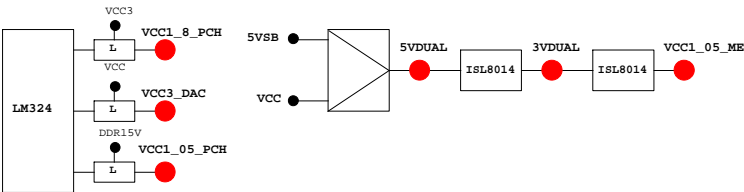
GIGABYTE™			
Title			
HDMI & USB			
Size	Document Number	Rev	
Custom	GA-H77-D3H-MVP	1.02	
Date:	Friday, April 06, 2012	Sheet	37 of 38

PCH GPIO LIST TABLE				
PIN NAME	PWR	Default	USAGE	NOTE
GP0	MAIN	H-Z	GPI -PECI_REQ	N/A
GP1/TACH1	MAIN		GPI ICH_FAN_TACH1	N/A
GP2/PIRQE#	MAIN		GPI -PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN		GPI -PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN		GPI -PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN		GPI -PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN		GPI ICH_FAN_TACH2	N/A
GP7/TACH3	MAIN		GPI ICH_FAN_TACH3	N/A
GP8	STBY	H	GPO GPIO8	P/U 8.2K 3VDUAL
GP9/OC5#	STBY		NATIVE OC5#	N/A
GP10/OC6#	STBY		NATIVE OC6#	N/A
GP11/SMBALERT#	STBY		NATIVE -SMBALERT	P/U 8.2K 3VDUAL
GP12	STBY	L	GPI LAN_PHY_PWR_CTRL	P/U 8.2K 3VDUAL
GP13	STBY	L	GPI GPIO13	P/U 8.2K 3VDUAL
GP14/OC7#	STBY		NATIVE OC7#	N/A
GP15	STBY	L	GPO GPIO15	N/A
GP16	MAIN		GPI -SKTOCC	P/U 8.2K VCC3
GP17/TACH0	MAIN		GPI ICH_FAN_TACH0	N/A
GP18	MAIN		NATIVE MB_ID0	P/D 8.2K GND
GP19	MAIN		GPI -LAN1_ISO	P/U 8.2K VCC3
GP20	MAIN		NATIVE LED_CTL	P/U 1K VCC3
GP21	MAIN		GPI VCC18_FCH_OV2	P/U 8.2K VCC3
GP22	MAIN	H-Z	GPI VCORE_OV3	P/U 8.2K VCC3
GP23	MAIN		NATIVE -LDRQ1	P/U 8.2K VCC3
GP24	STBY	L	GPO TLS	P/U 8.2K 3VDUAL
GP25	STBY		NATIVE -CPU_STOP	P/U 8.2K 3VDUAL
GP26	STBY		NATIVE -ACZ_DET	P/U 8.2K 3VDUAL
GP27	STBY	H	GPO GPIO27	P/U 8.2K 3VDUAL
GP28	STBY	H	GPO GPIO28	P/U 8.2K 3VDUAL
GP29	STBY	L	GPI GPIO29	N/A
GP30	STBY	H-Z	GPI S_PWR_ACK	P/U 100K 3VDUAL
GP31	STBY	H-Z	GPI N/A(Reverse)	P/U 8.2K VCC3
GP32	MAIN	H	GPO MB_ID1	P/D 8.2K GND
GP33	MAIN	H	GPO LOAD-LINE	P/U 1K VCC3
GP34	MAIN	H-Z	GPI -PCI_STOP	P/U 8.2K VCC3
GP35	MAIN	L	GPO GPIO35	P/U 8.2K VCC3
GP36	MAIN		GPI -LAN1_DSM	P/U 8.2K VCC3
GP37	MAIN		GPI N/A	P/U 8.2K VCC3
GP38	MAIN	H-Z	GPI VCORE_OV2	P/U 8.2K VCC3
GP39	MAIN	H-Z	GPI -LAN_DSM	P/U 8.2K VCC3
GP40	STBY		NATIVE OC1#	N/A
GP41	STBY		NATIVE OC2#	N/A
GP42	STBY		NATIVE OC3#	N/A
GP43	STBY		NATIVE OC4#	N/A
GP44	STBY	L	NATIVE N/A	P/U 8.2K 3VDUAL
GP45	STBY		NATIVE -LPCPME	P/U 8.2K 3VDUAL
GP46	STBY	L	NATIVE PWR_LED	P/U 8.2K 3VDUAL
GP47	STBY		NATIVE PSI_LED	P/U 8.2K 3VDUAL
GP48	MAIN	H-Z	IN EN_PWM	P/U 8.2K VCC3
GP49	MAIN	H-Z	IN VCC18_OV1	P/U 8.2K VCC3
GP50	MAIN		NATIVE -REQ1	P/U 2.2K VCC
GP51	MAIN	H	NATIVE -GNT1	N/A
GP52	MAIN		NATIVE -REQ2	P/U 2.2K VCC
GP53	MAIN	H	NATIVE -GNT2	N/A
GP54	MAIN		NATIVE -REQ3	P/U 2.2K VCC
GP55	MAIN	H	NATIVE -GNT3	N/A
GP56	STBY		NATIVE N/A(Reverse)	P/U 8.2K 3VDUAL
GP57	STBY	H-Z	IN VCORE_OV1	P/U 8.2K 3VDUAL
GP58	STBY	H-Z	NATIVE F_USB_OC	P/U 8.2K 3VDUAL
GP59	STBY		NATIVE USB_OC0#	N/A
GP60	STBY	H-Z	NATIVE N/A(Reverse)	P/U 8.2K 3VDUAL
GP61	STBY	L	NATIVE -SUSTAT	N/A
GP62	STBY	L	NATIVE SUSCLK	N/A
GP63	STBY	L	NATIVE GPIO63	N/A
GP64	MAIN	L	NATIVE CLKOUTFLEX0	N/A
GP65	MAIN	L	NATIVE CLKOUTFLEX1	N/A
GP66	MAIN	L	NATIVE CLKOUTFLEX2	N/A
GP67	MAIN	L	NATIVE CLKOUTFLEX3	N/A
GP72	STBY	H-Z	NATIVE VCORE_OV4	P/U 8.2K 3VDUAL
GP73	STBY		NATIVE 1_05V_OV1	P/U 8.2K 3VDUAL
GP74	STBY	H-Z	NATIVE 1_05V_OV2	P/U 8.2K 3VDUAL
GP75	STBY	H-Z	NATIVE N/A(Reverse)	P/U 8.2K 3VDUAL

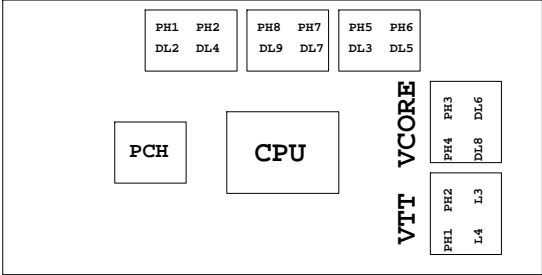
Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRXL/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSSO0	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSSI1	SB_LED1_C	
PD4/GP74/BUSSI2	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSSI0	NB_LED3_C	
GP22/SCK	LOW_PWR_1	
VID05/GP27/SIN2	LOW_PWR_2	
PCIRST2#/GP11	-PWRST1	
PCIRST1#/GP12	-PWRST2	
3VSBSW#/GP40	CSI_F0	BSEL166_1
SUSC#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VID00/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSSO1	MB_ID3	
PD7/GP77/BUSSO2	MB_ID4	
AFD#/GP86/SMBD_R	3x PIN	FST_2X8
INIT#/GP85/SMBD_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VID01/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMBD_M	DDR_LED3_C	
PWRON#GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRXL2/GP16	-THERM	
VID04/GP26/SOUT2	DDR18V_PH2_EN	
VID02/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VID06/GP17/RI2#	1_1V_PH_EN	
VID07/JP6/DTR2#	JP6	
PD5/GP75/BUSSO0	SB_LED3_C	



PWM各相位的擺法如下：



BIOS超電壓對應表：

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Terminatio
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

散熱模組料號：

8IBP:
1.12SP2-01A001-Y1R/Y2R
2.12SP2-01A001-Z1R/Z2R
(HIBRID模組)包材階

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH